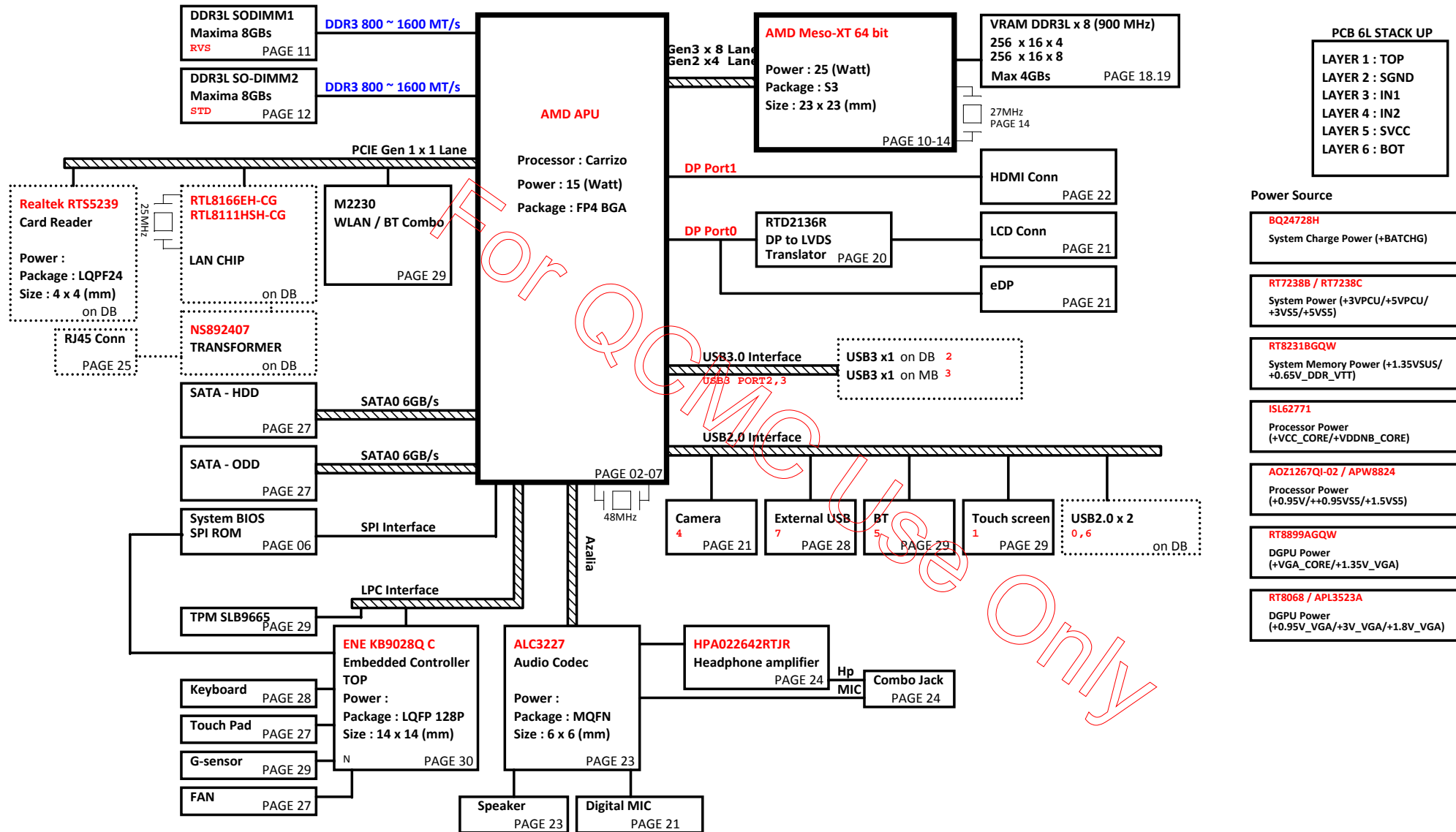
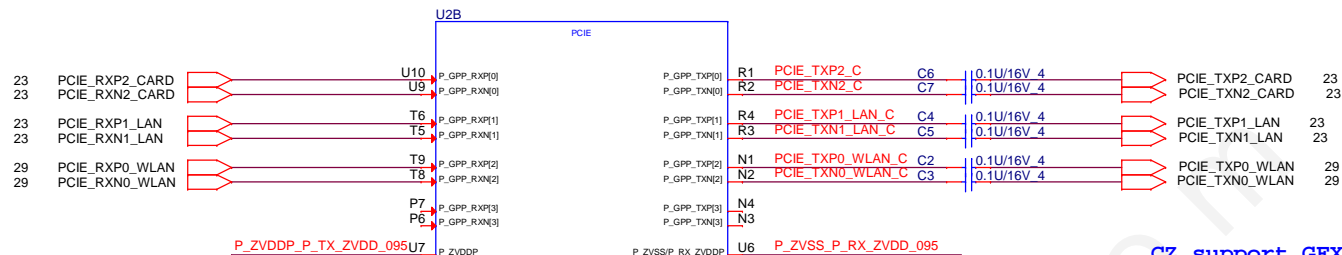


Chocolate_AMD Carrizo(L) DIS/UMA (14.0"/15.6"/17.3")

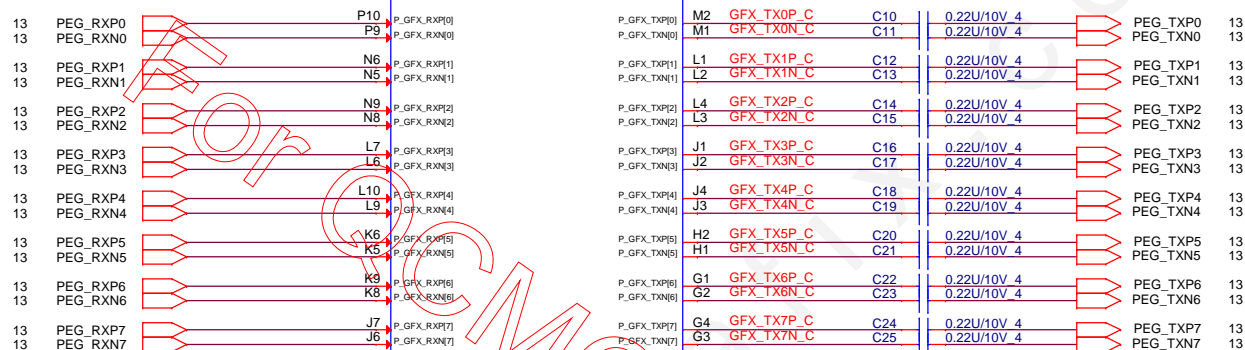
01





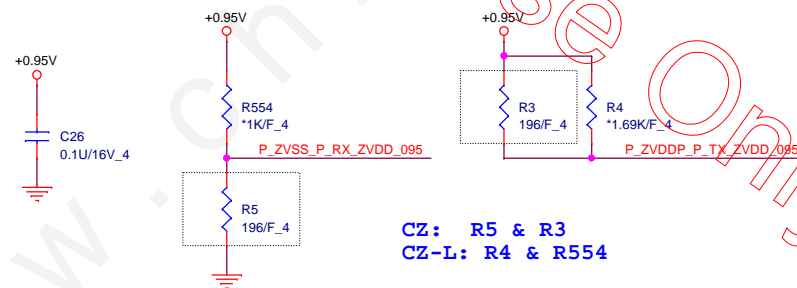
CZ support GFX 0~7 & Gen3
CZ-L only support GFX 0~3 & Gen2

Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4102K1B03



For DIS GPU

FP4 REV 1.0



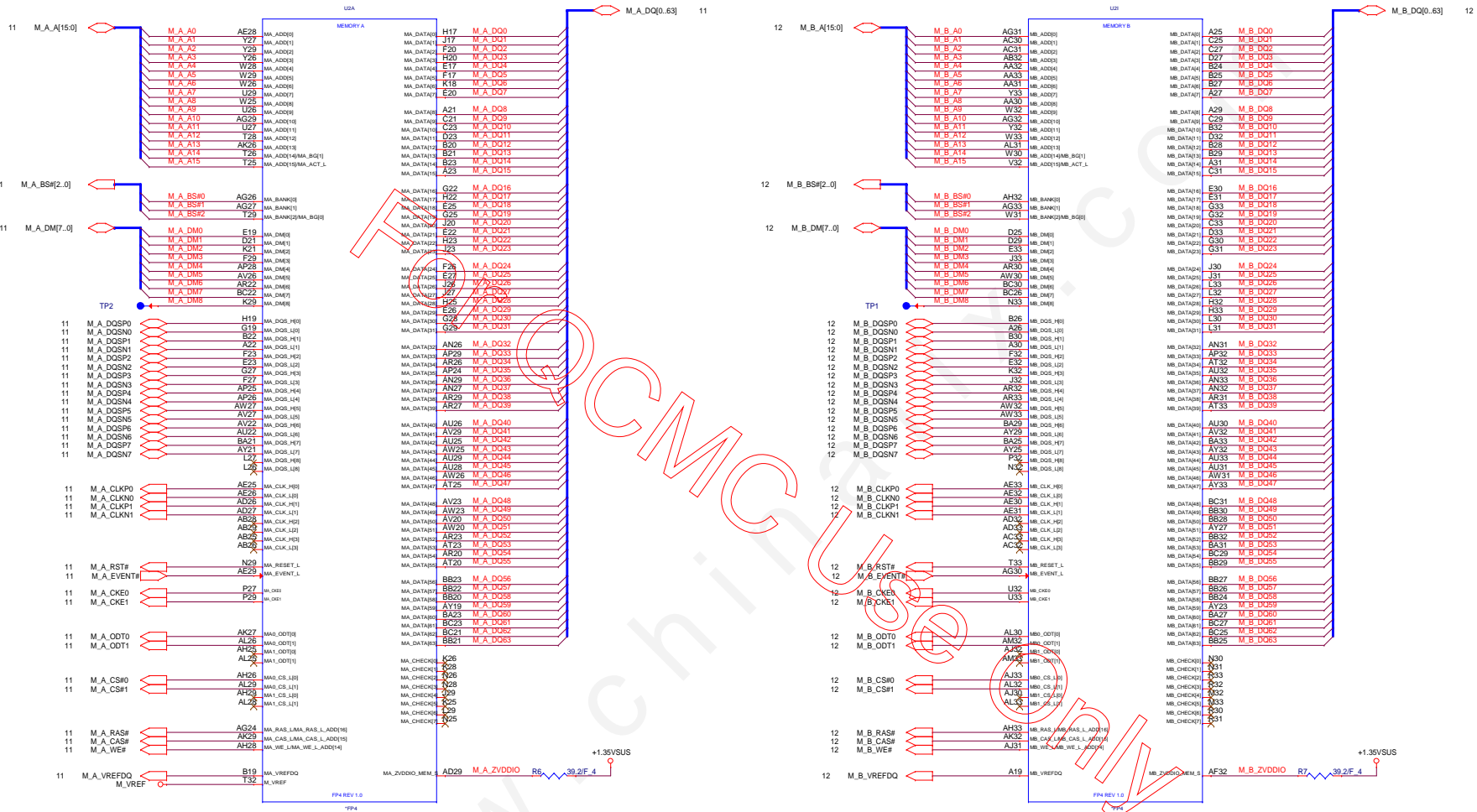
CZ: R5 & R3
CZ-L: R4 & R554



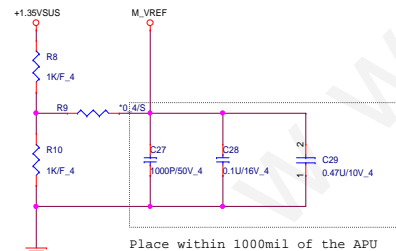
PROJECT : X21
Quanta Computer Inc.

Size	Document Number	Rev
	Carrizo 1/7 (PCIE)	1A

Date: Tuesday, February 03, 2015 Sheet of 43



CR-I only channel B



BOARD ID TABLE

Model	ID0	ID1	ID2	ID3	ID4	ID5	ID6	ID7
CZ 14" UMA	0	0	0	0	0	0	0	0
CZ 14" SG	1	0	0	0	0	0	0	0
CZ 15" UMA	0	1	0	0	0	0	0	0
CZ 15" SG	1	1	0	0	0	0	0	0
CZ 17" UMA	0	0	1	0	0	0	0	0
CZ 17" SG	1	0	1	0	0	0	0	0

BOARD ID SETTING

Board ID 0	Definition
0	UMA
1	SG

Board ID [2:1]	Definition
00	14"
01	15"
10	17"

Board ID [4:3]	Definition
00	Pavilion
01	Reserve
10	Reserve

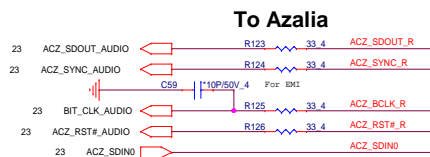
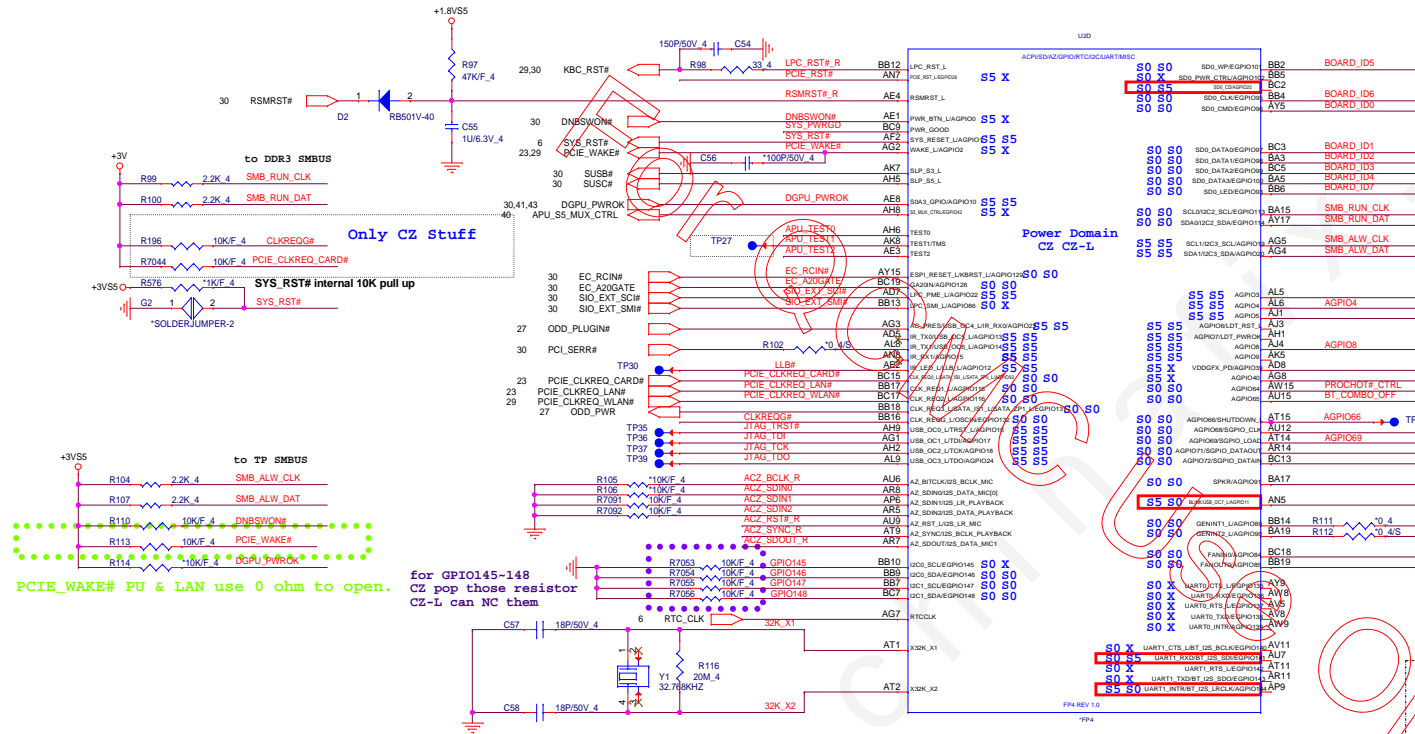
Board ID [5]	Definition
0/1	CZ/CZ-L

Board ID [7:6]	Definition
00	Reserve

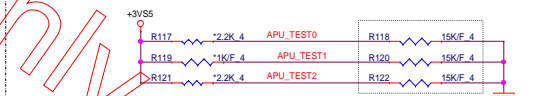
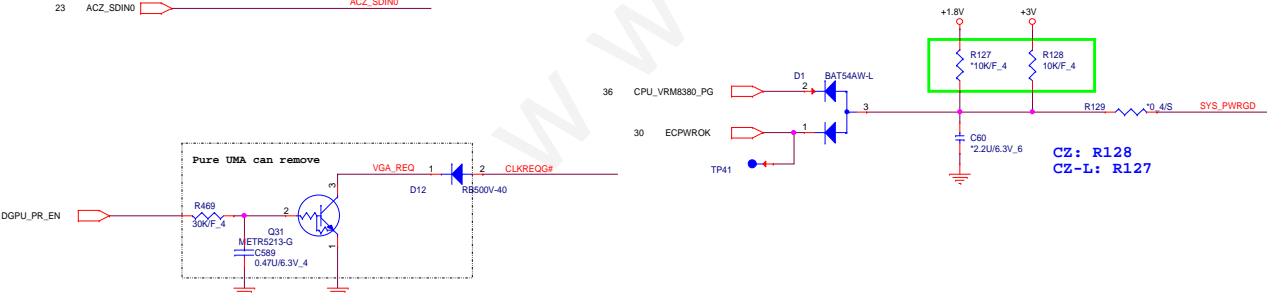
05



12/3: modify schematic for cost down space



SYS PWRGD

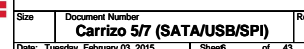


Follow AMD checklist 53537_1_03 suggestion to stuff R118/R120/R122

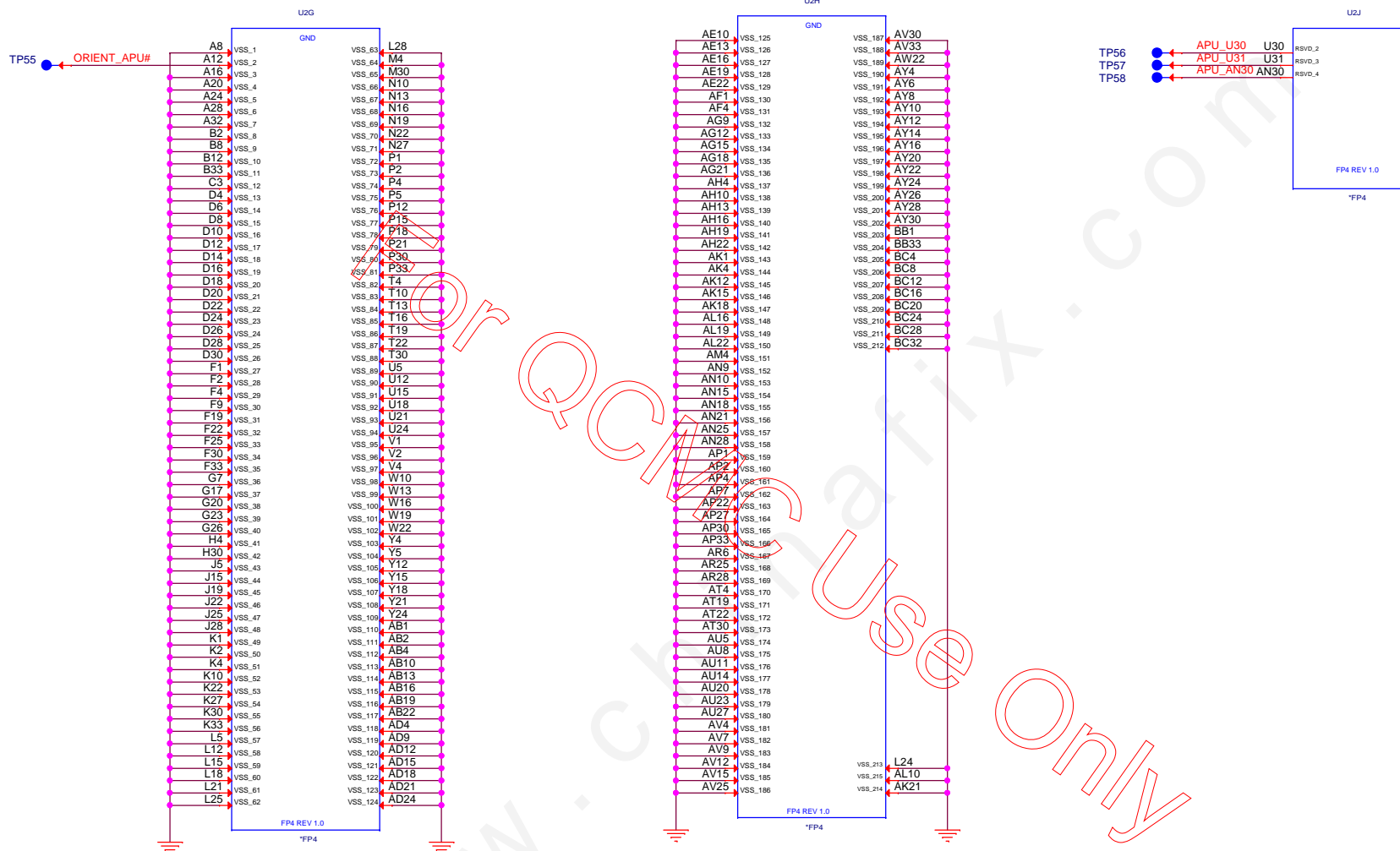
TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled

PROJECT : X21
Quanta Computer Inc.

Size Document Number
Carrizo 4/7 (GPIO/AZ/UARTH)
Rev 1A
Date: Tuesday, February 03, 2015 Sheet6 of 43







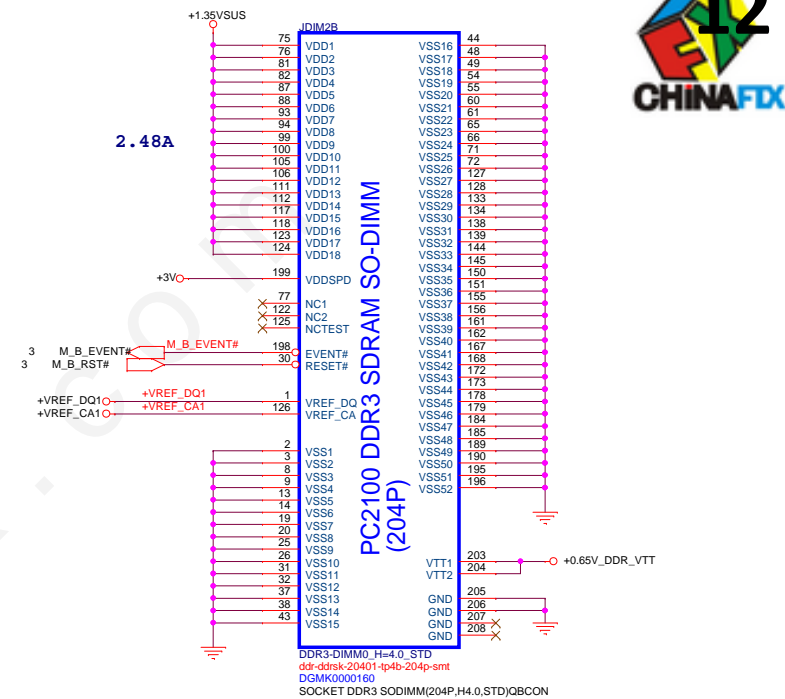
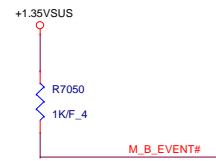
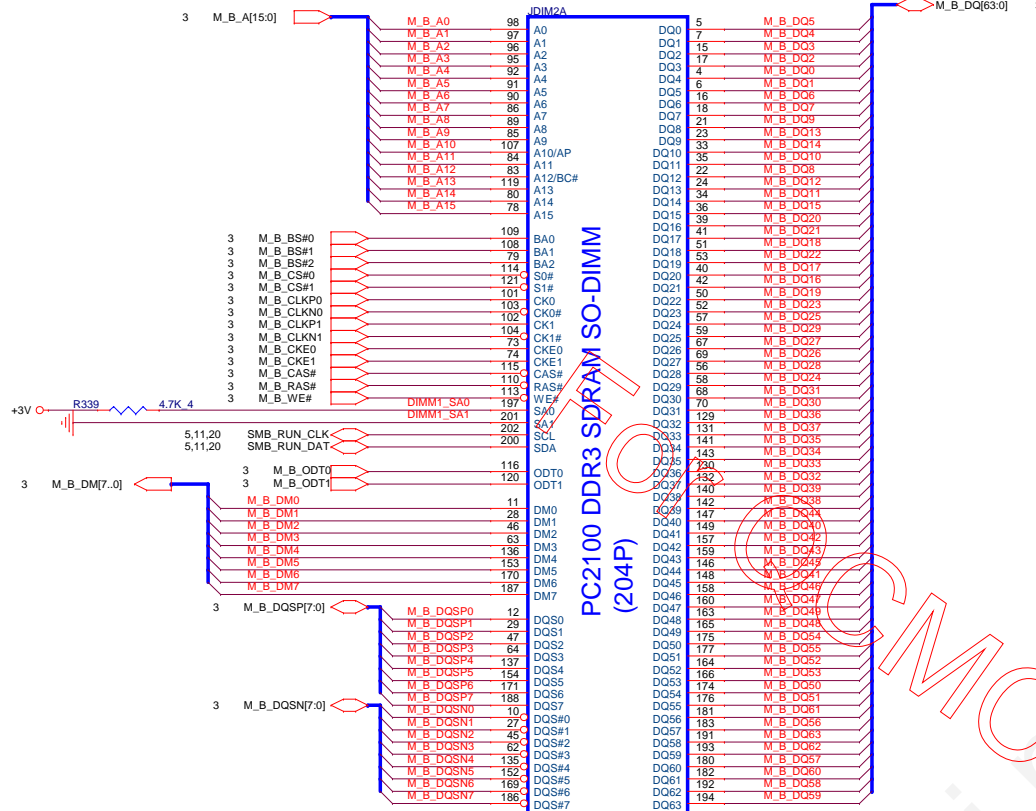
For QCMC Use Only

www.chinafix.com



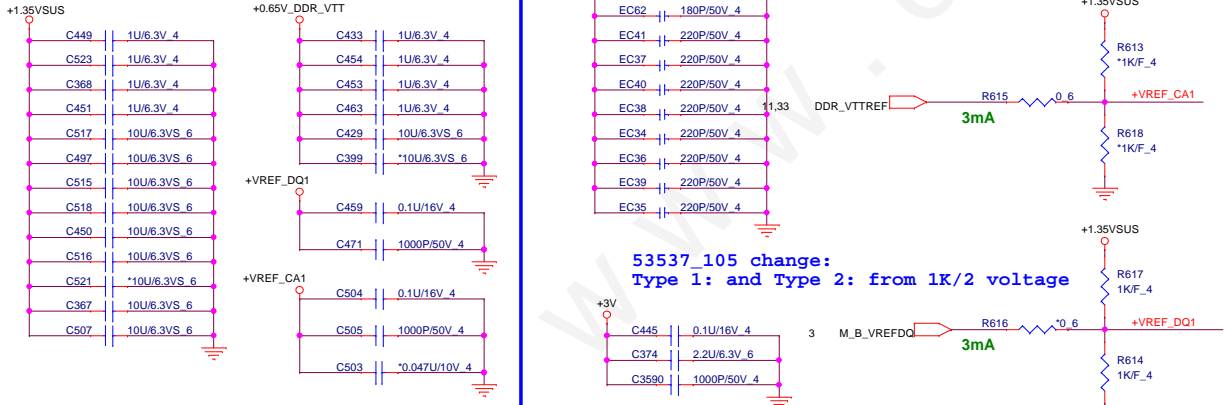
For QCMC Use Only

www.chinafix.com



DDR3-DIMM0_H=4.0 STD
ddr-ddrsk-20401-tp4b-204p-smt
DGMK0000160
SOCKET DDR3 SODIMM(204P,H4.0,STD)QBON

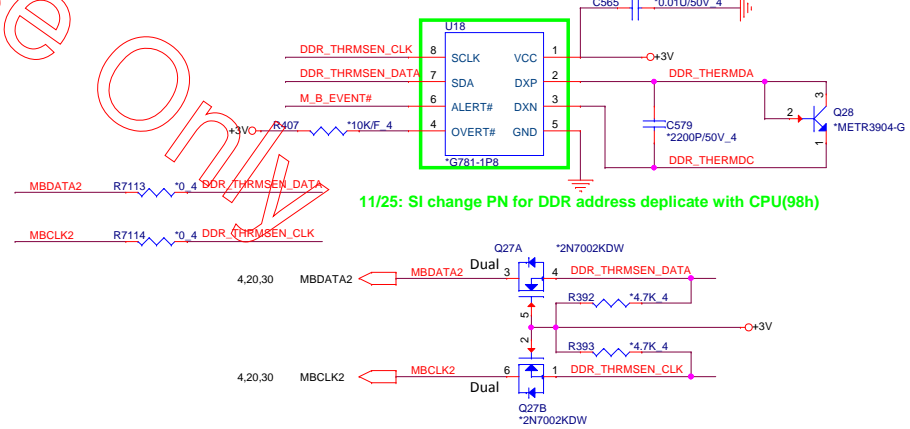
Place these Caps near So-Dimm1.



53537_105 change:
Type 1: and Type 2: from 1K/2 voltage

Local Thermal Sensor

DDR3 Thermal Sensor
Main:AL000781039 G781-1P8(9Ah)

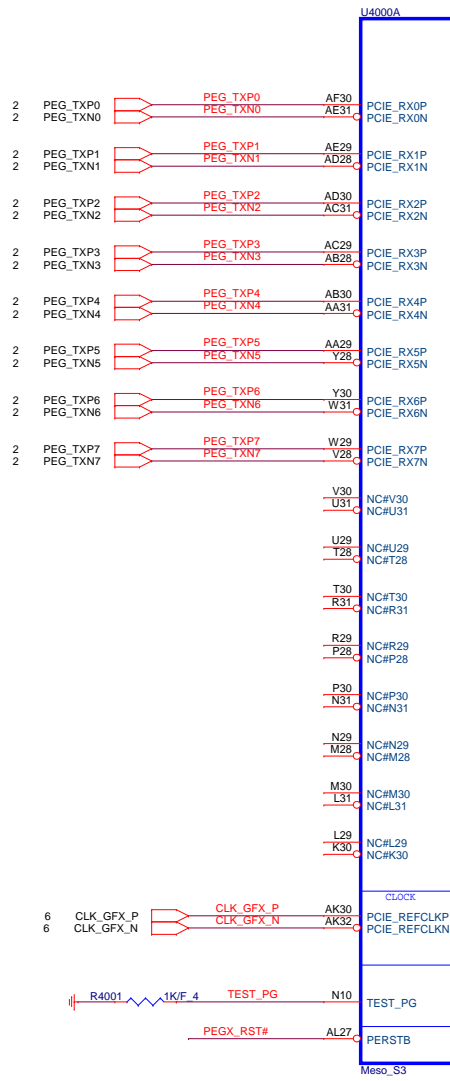


11/25: SI change PN for DDR address decapicate with CPU(98h)

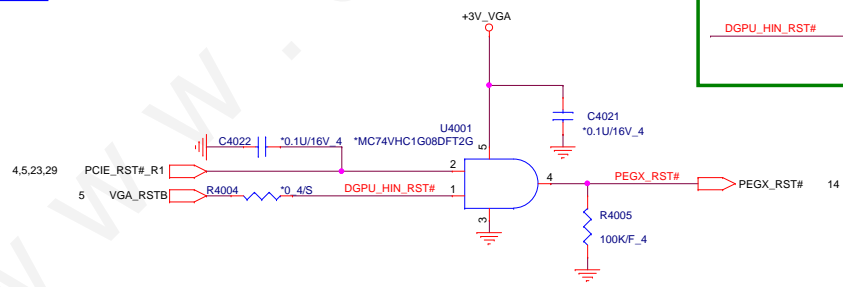
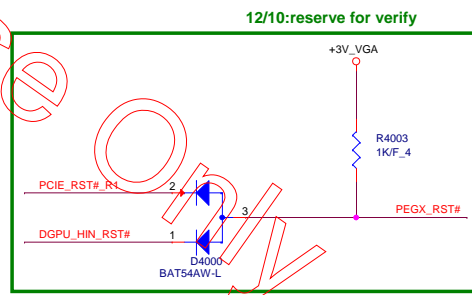
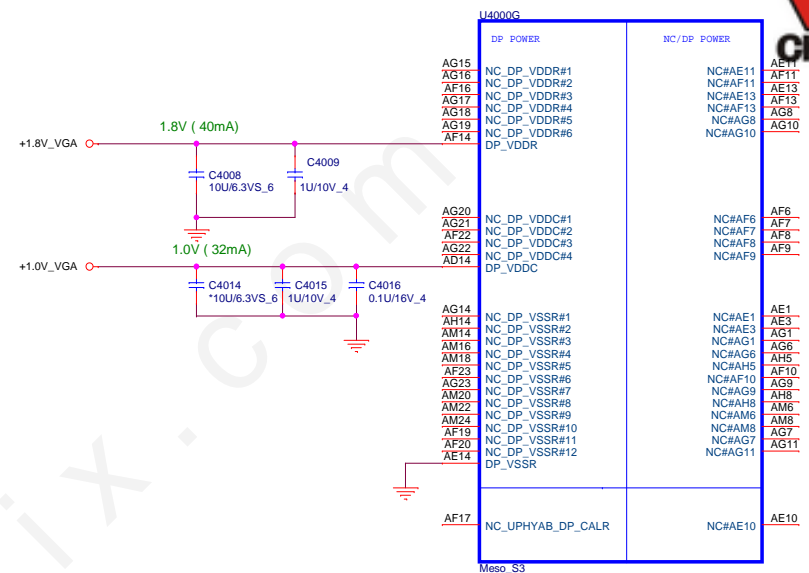
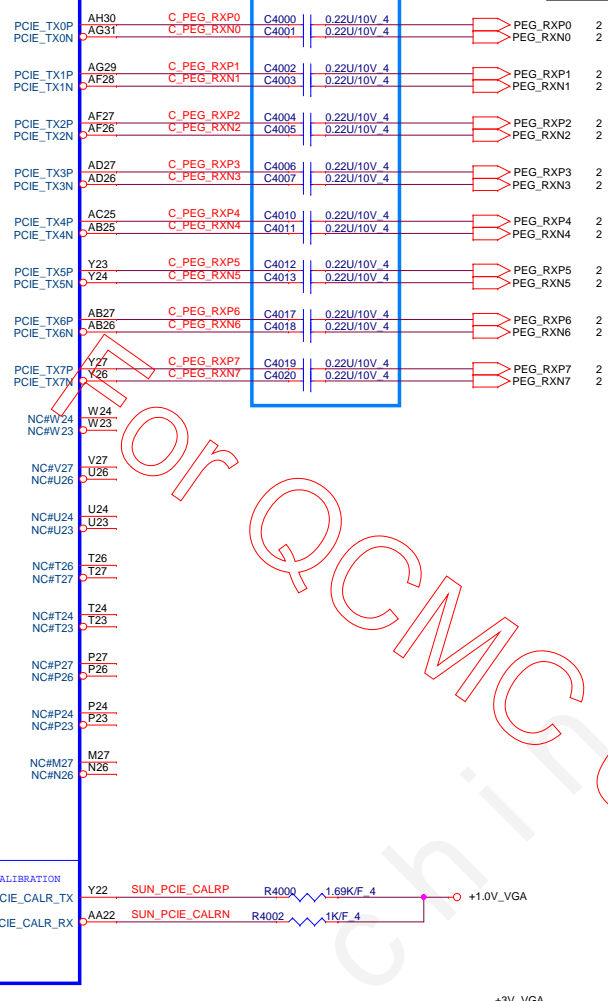
Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4102K1B03

9/2: CZ use 0.22u(Gen 3) ; CZ-L use 0.1u(Gen 2)



PCI EXPRESS INTERFACE



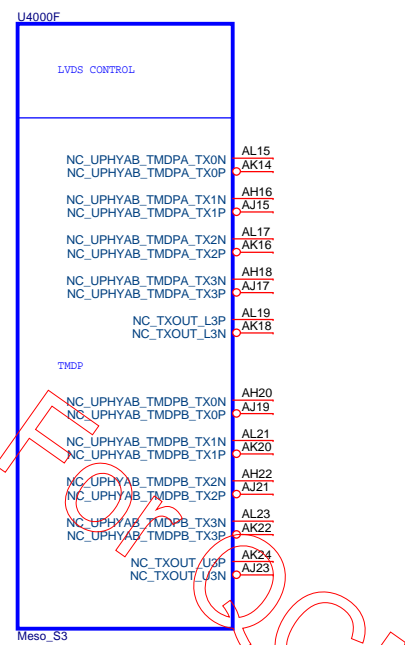
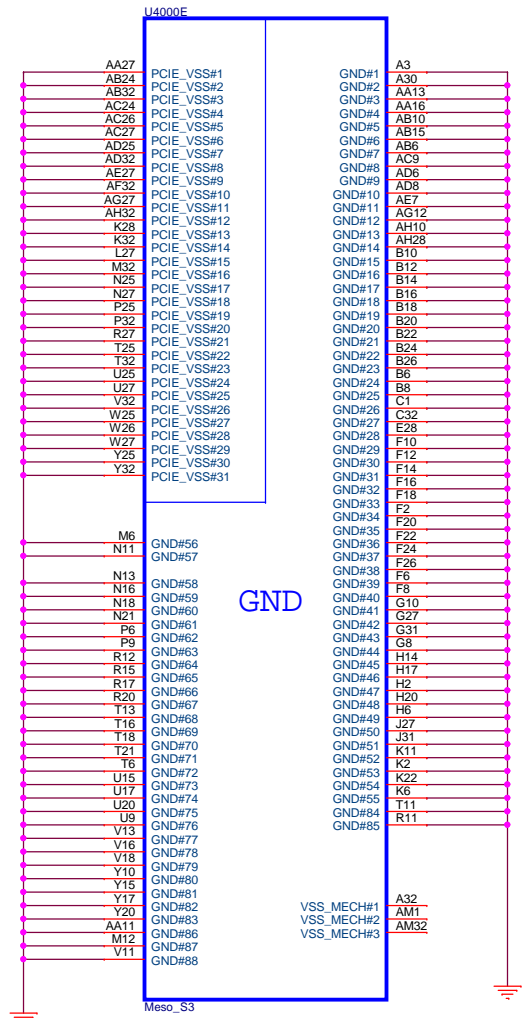


Capacitor Lookup Table		Resistor Divider Lookup Table		
C (nF)	Bits(5,4)	R _{pu} (Ohm)	R _{pd} (Ohm)	Bits(3,2,1)
680	00	NC	4750	000
82	01	8450	2000	001
10	10	4530	2000	010
NC	11	6980	4990	011
		4530	4990	100
		3240	5620	101
		3400	10000	110
		4750	NC	111

ready stuff

review result

For AMD tuning
timing purpose



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/W/histler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYS	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

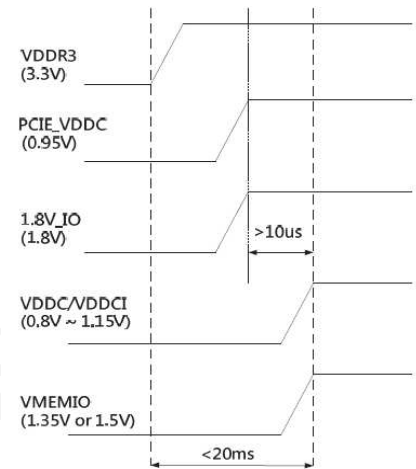
NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

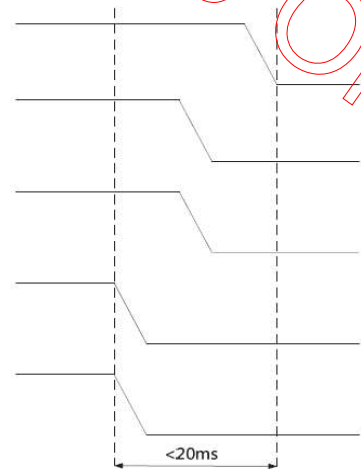
GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE

POWER UP

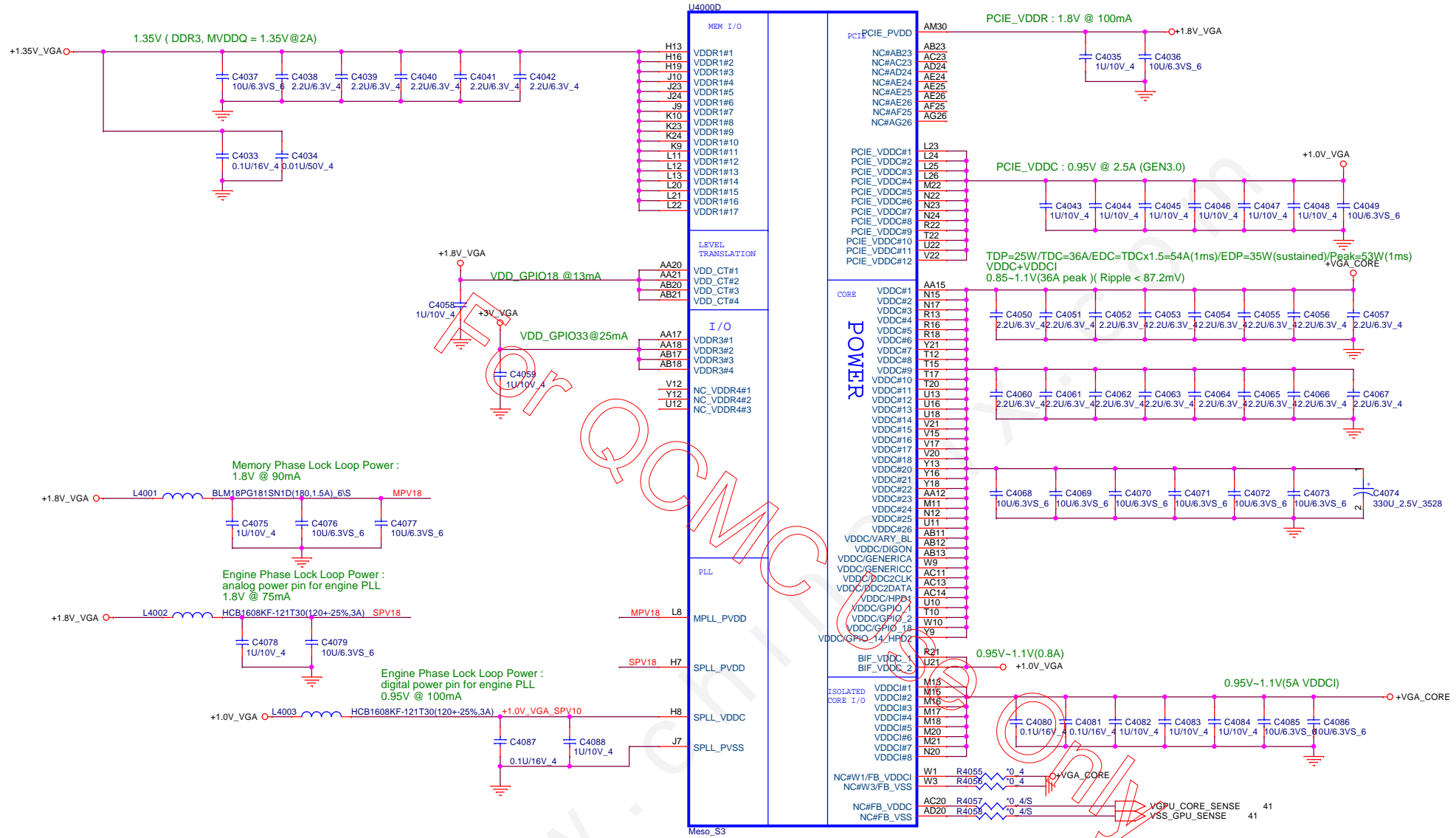


POWER DOWN



PROJECT : Y23
Quanta Computer Inc.

Size	Document Number	Rev
	TOPAZ_S3_GND/LVDS/Strap	1A
Date:	Tuesday, February 03, 2015	Sheet 15 of 43

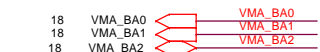


+1.35V_VGA 17,18,40,41
 +1.8V_VGA 13,14,40,41,43
 +1.0V_VGA 13,40,43
 +VGA_CORE 40,41,42

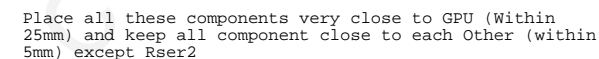
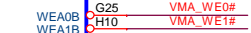


PROJECT : Y23
Quanta Computer Inc.

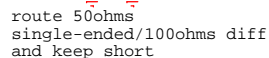
Size	Document Number	Rev
	TOPAZ S3 Power	1A
Date:	Tuesday, February 03, 2015	Sheet 16 of 43

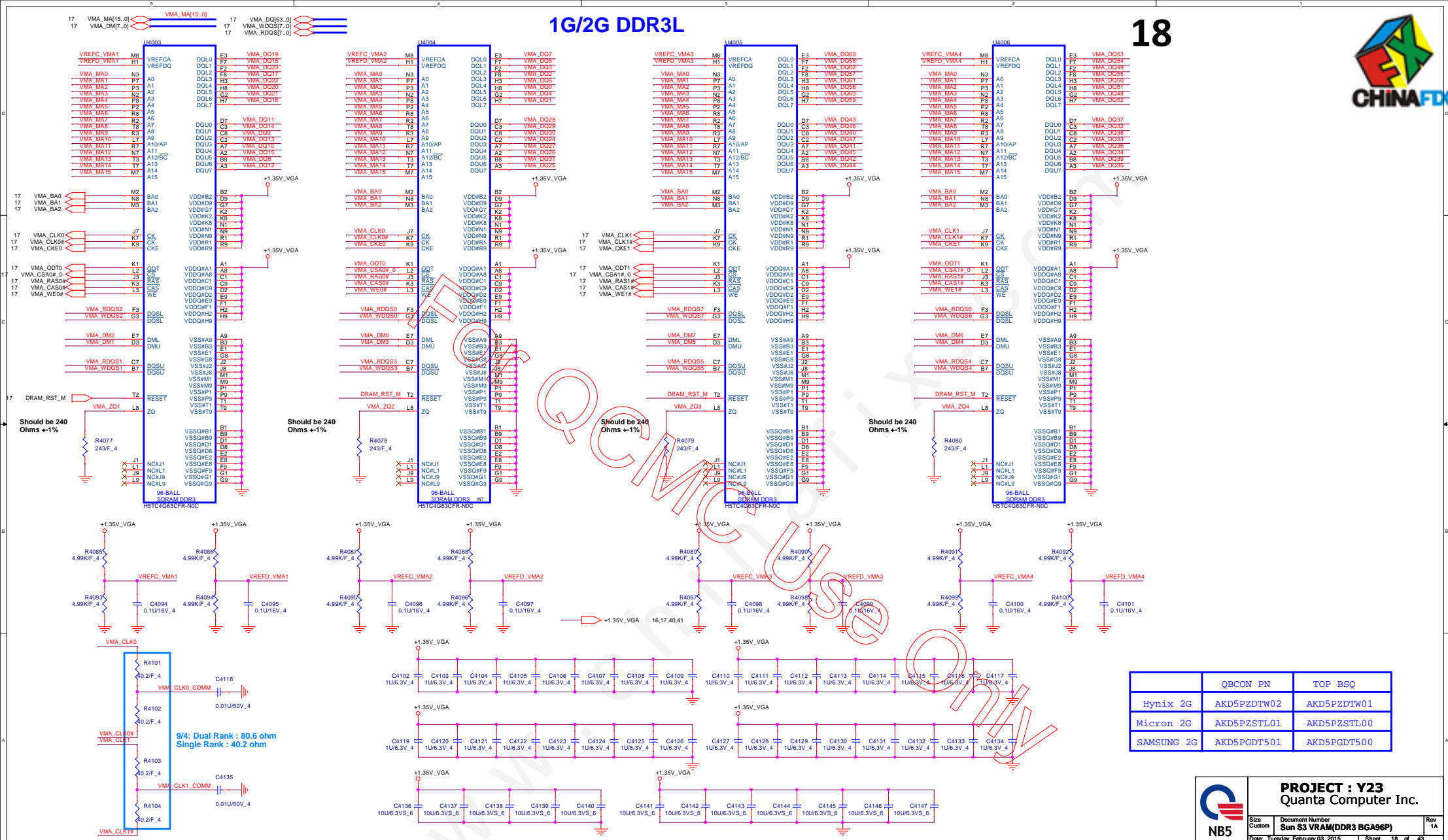


support 1Gbit
VRAM (64M X 16)




This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

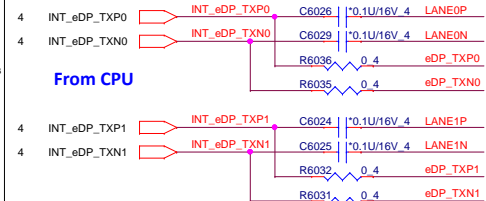
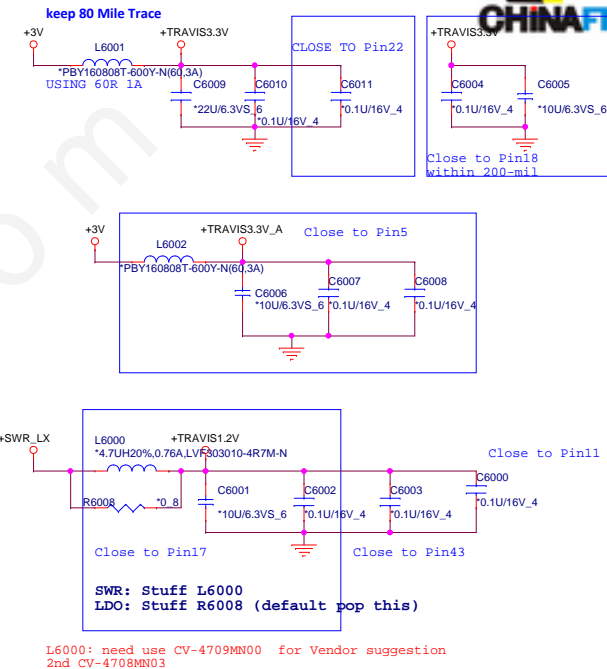
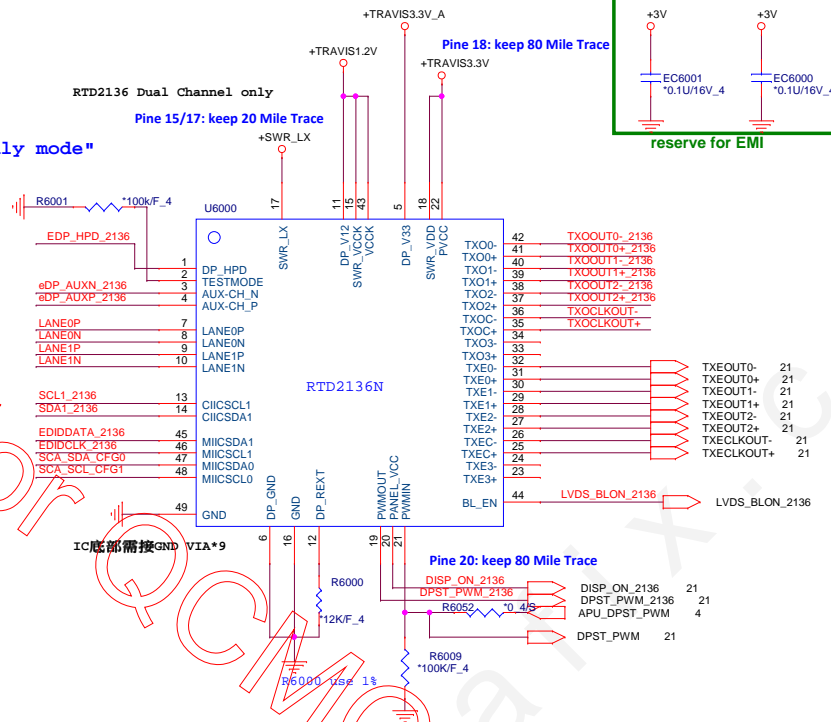




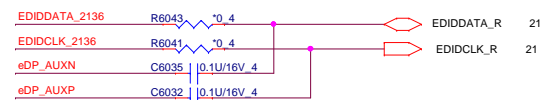
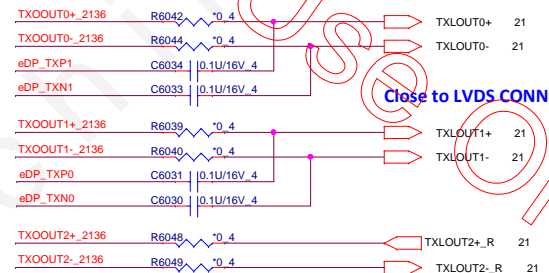
For QCMC Use Only

 NB5	PROJECT : Y23 Quanta Computer Inc.	Rev 1A
Size Custom	Document Number Sun S3 VRAM(DDR3 BGA96P)	
Date: Tuesday, February 03, 2015		Sheet 19 of 43

19

[illegible]

For EDP Only: stuff Resistor
For LVDS only stuff Cap



For EDP Only: stuff Cap
For LVDS only stuff Resistor

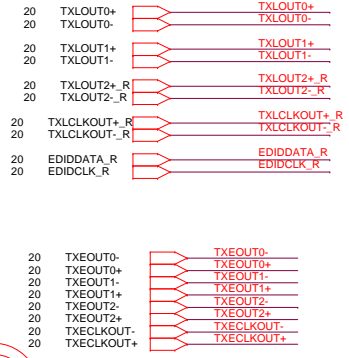
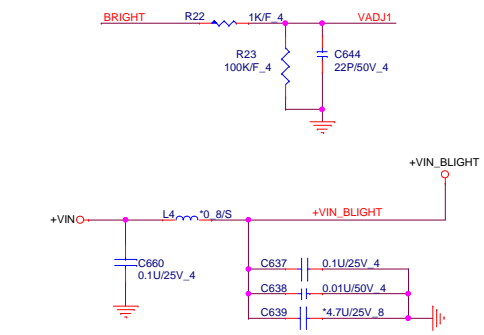
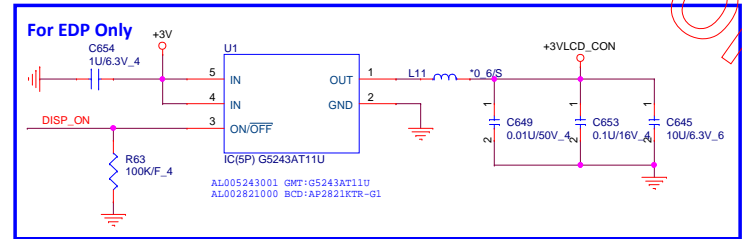
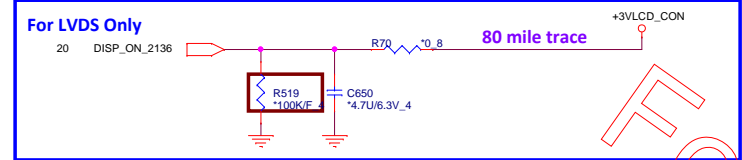
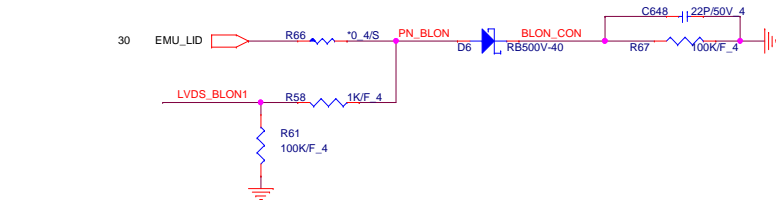
4,5,6,7,11,12,21,22,23,24,27,28,29,30,36,38,40 +3V 



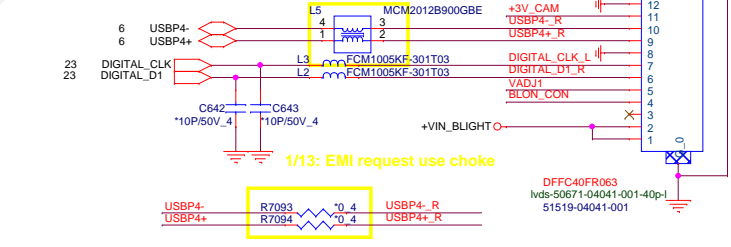
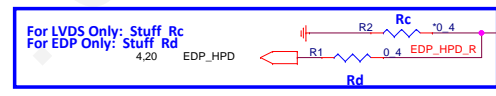
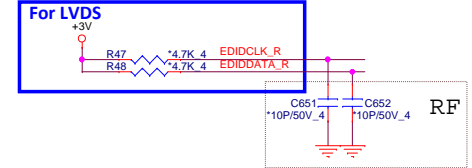
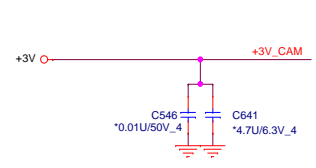
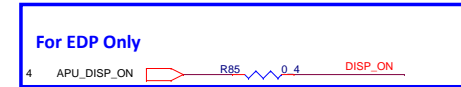
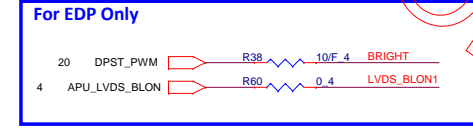
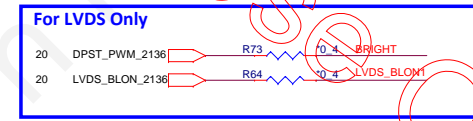
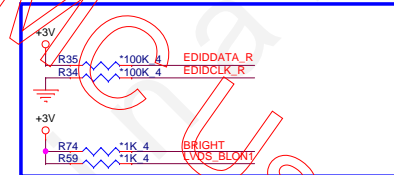
PROJECT : X21
Quanta Computer Inc.

Size Custom	Document Number LVDS converter RTD2136	Rev 1A
Date: Tuesday, February 03, 2015		Sheet 20 of 43

LVDS conn.
14'' & 15'' only eDP panel SKU , 17'' have both LVDS & eDP SKU

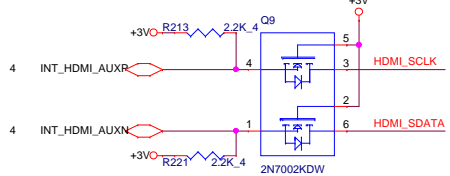


For EDP Only(DG show AUX don't require PU/D)

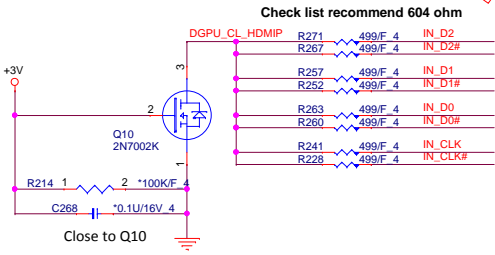
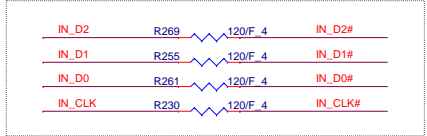


4,5,6,7,11,12,20,22,23,24,27,28,29,30,36,38,40
25,27,31,32,33,35,37,39,40,41,42

HDMI SMBus Isolation

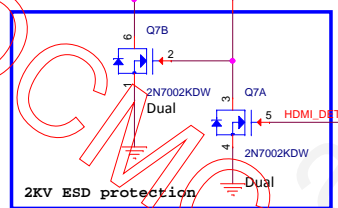


Close to HDMI connector

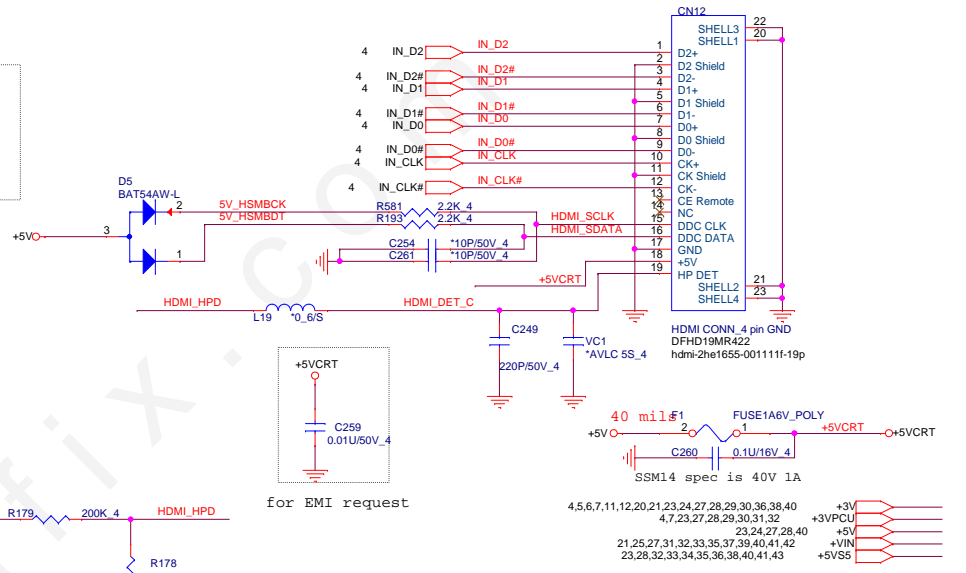


Check list recommend 604 ohm

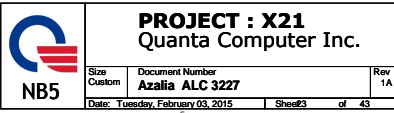
HDMI HPD SENSE

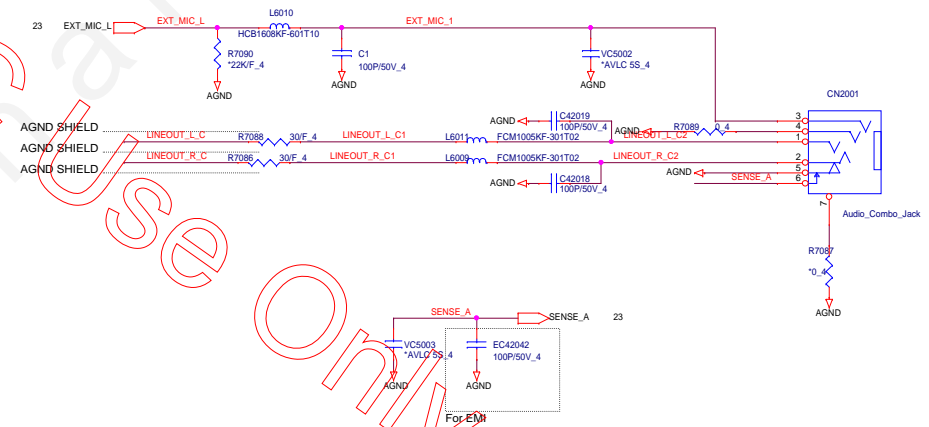


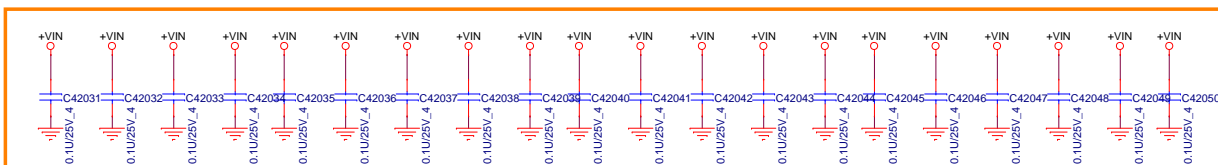
2KV ESD protection



for EMI request

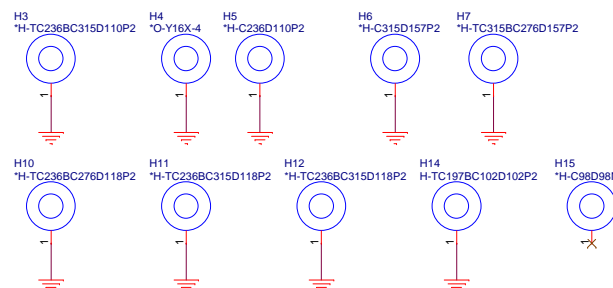
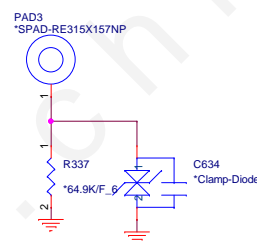
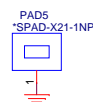
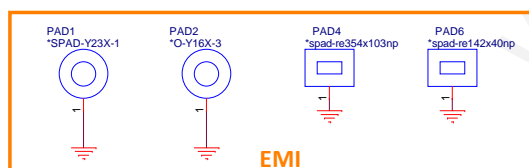
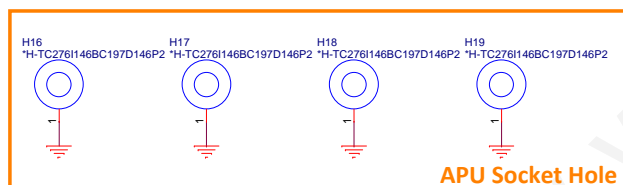
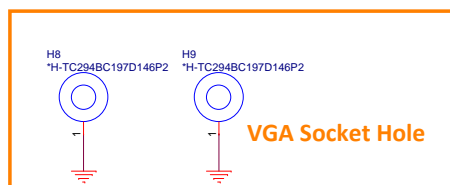






Place on 19V path

For QCMC Use Only

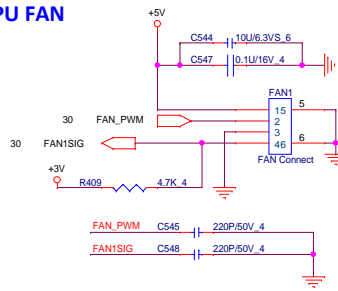


Nut for WLAN

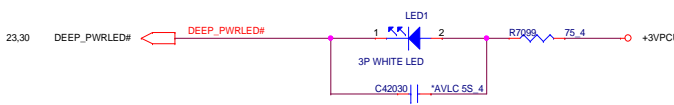
For QCMC Use Only

Power Button Connector (move to DB)

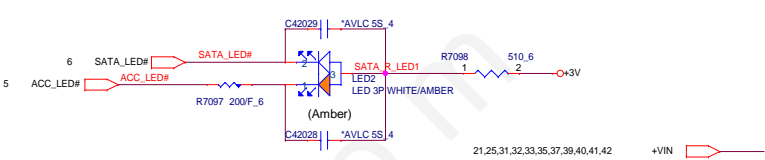
CPU FAN



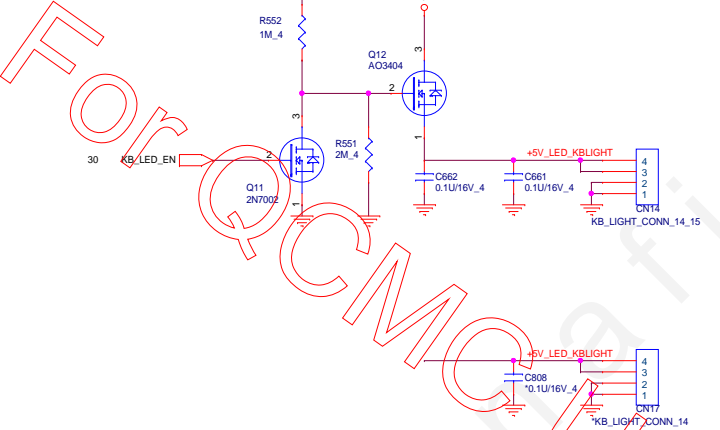
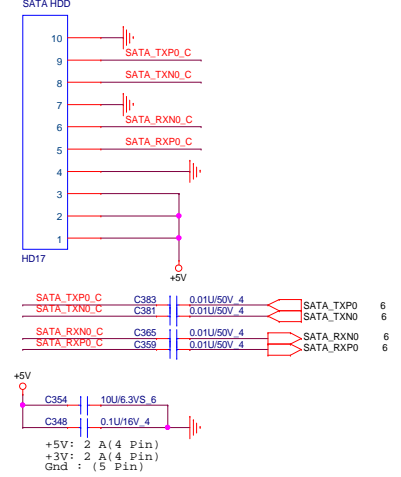
PWR LED



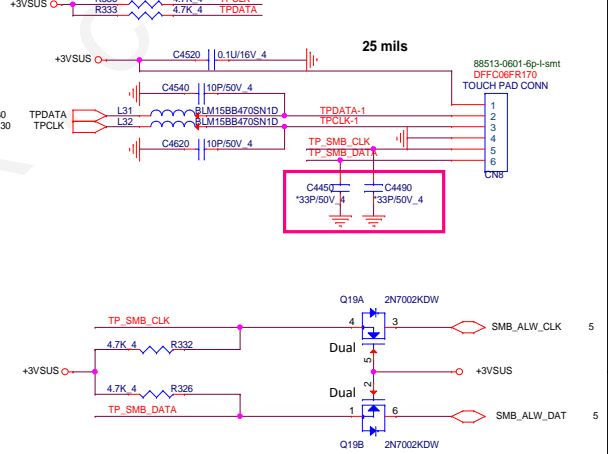
SATA LED



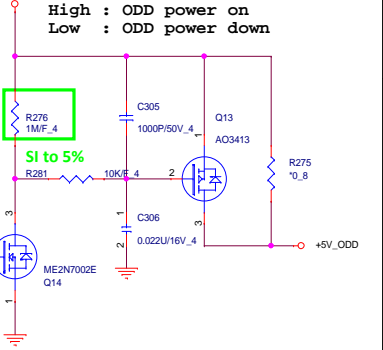
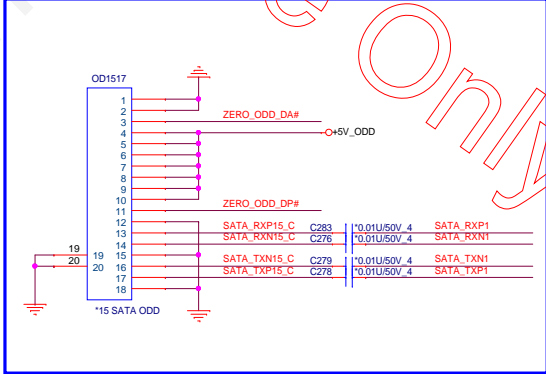
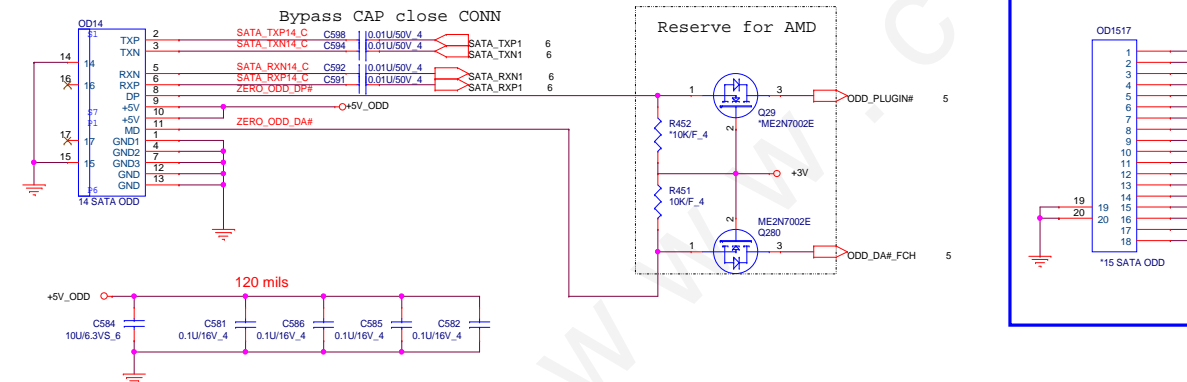
SATA HDD Connector(Cable type)



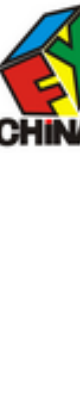
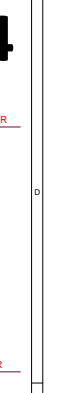
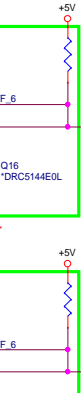
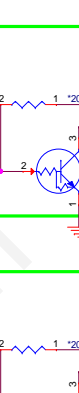
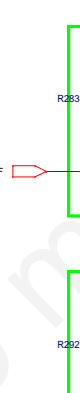
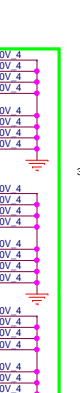
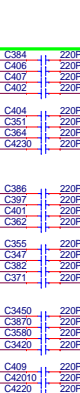
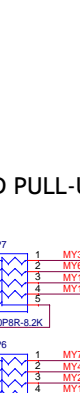
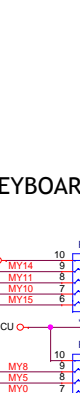
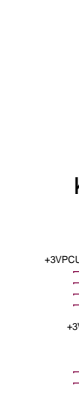
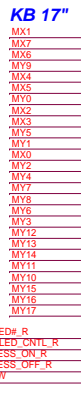
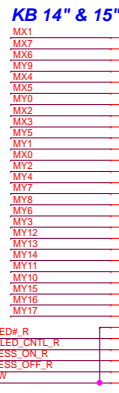
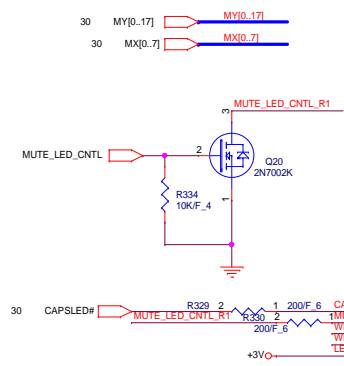
Touch Pad



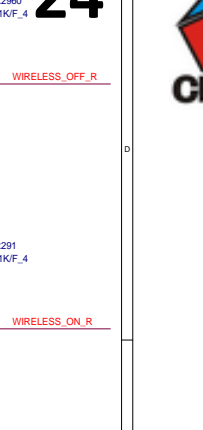
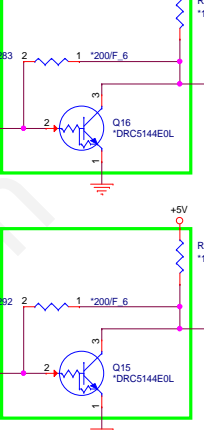
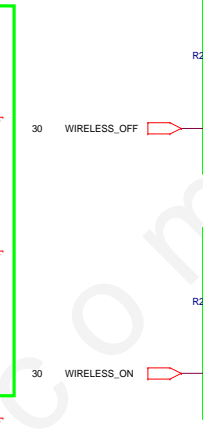
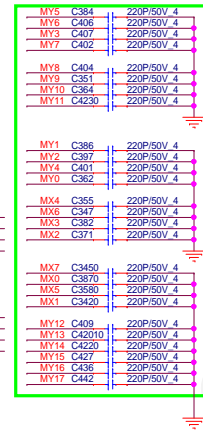
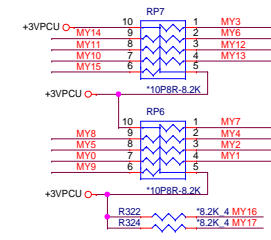
SATA ODD CONNECTOR



KEYBOARD Con.



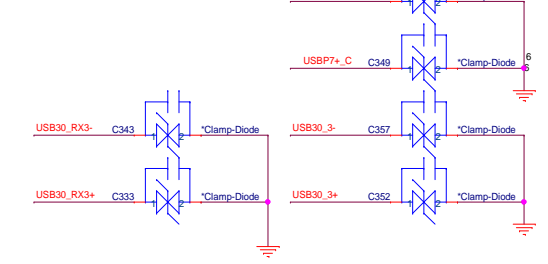
KEYBOARD PULL-UP



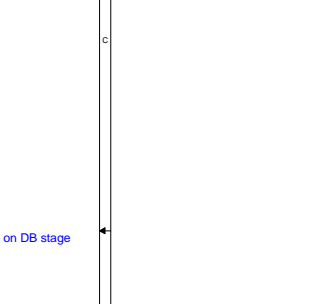
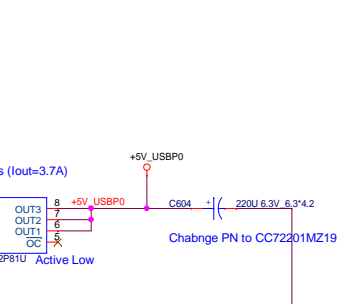
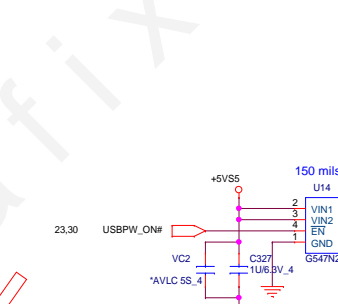
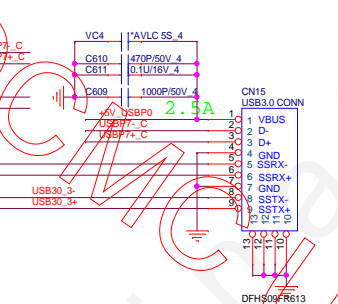
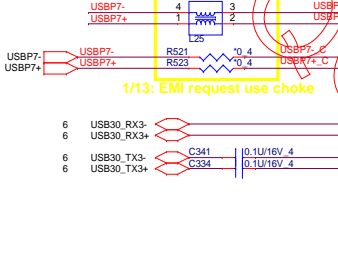
24



USB 2.0/3.0 Combo



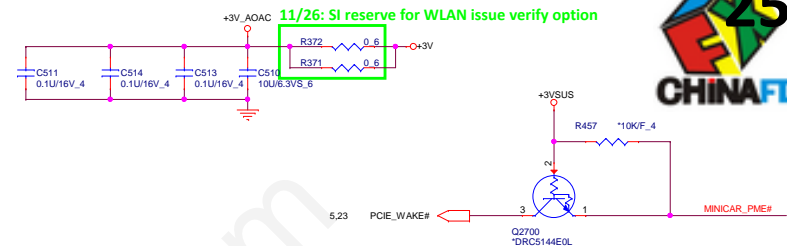
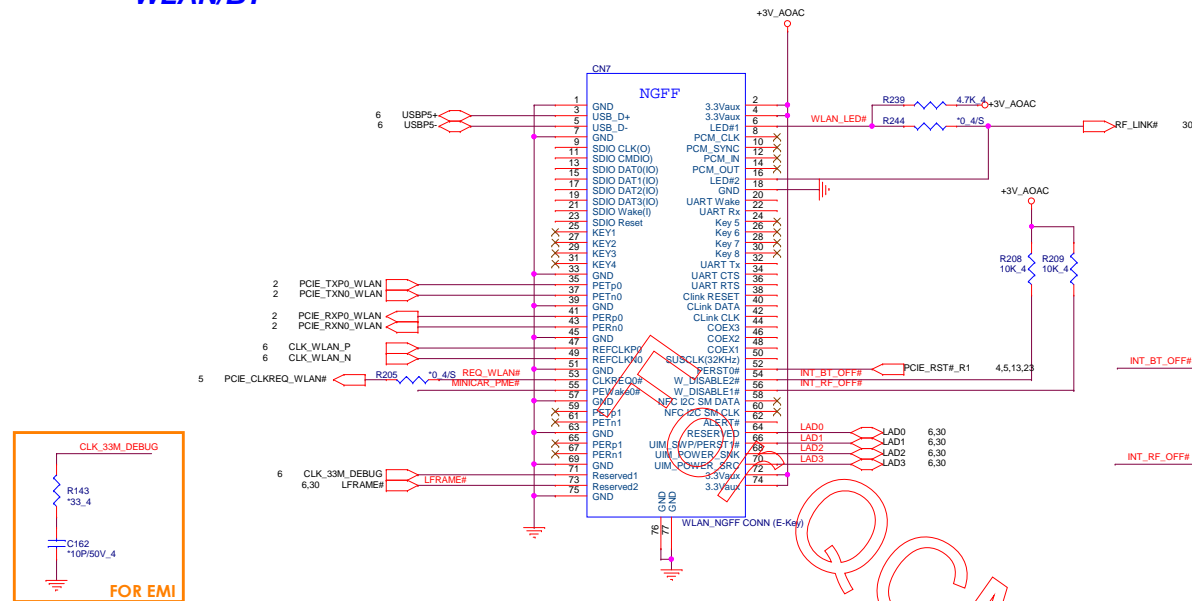
EMI: if charger IC no use, pop this choke



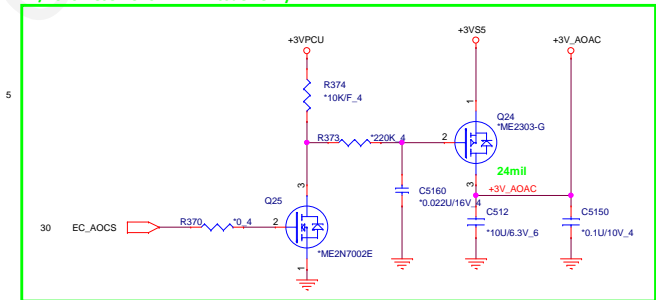
23,32,33,34,36,38,40,41,43
4,7,23,27,29,30,31,32

+5V/S5
+3VPCU

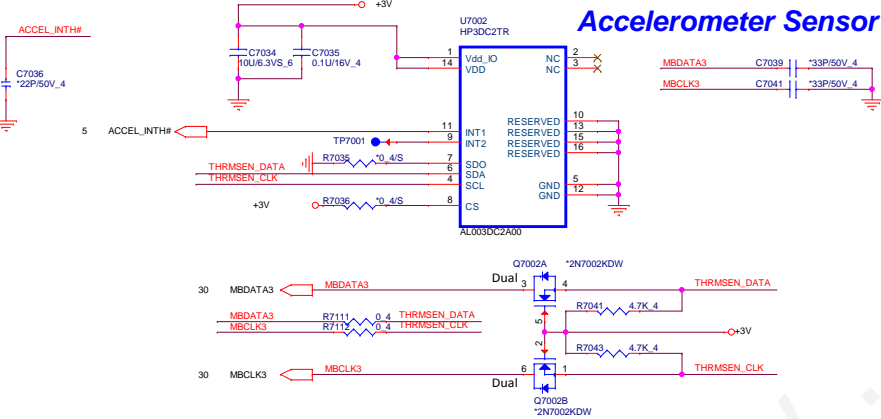
WLAN/BT



11/26: SI reserve for WLAN issue verify

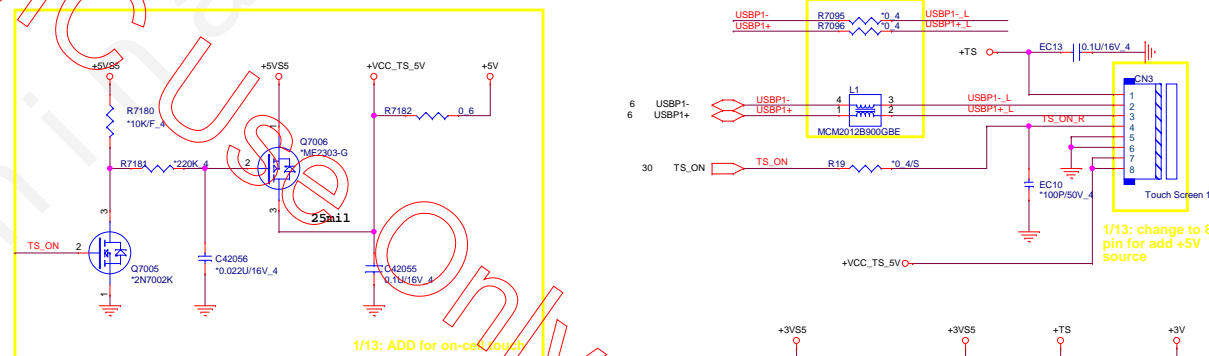


Accelerometer Sensor



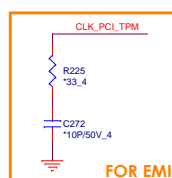
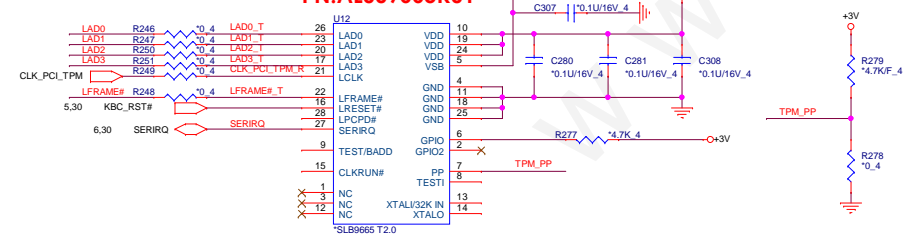
Touch screen

1/13: EMI request use choke

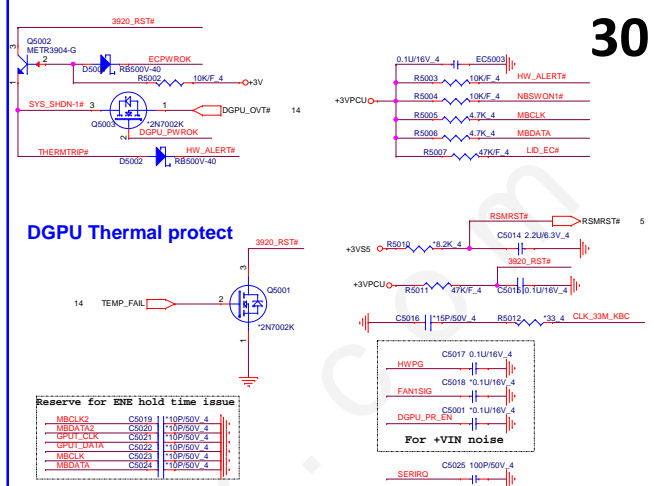


TPM (2.0)

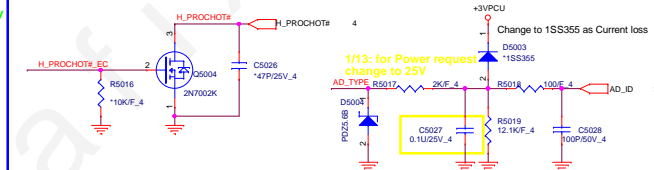
PN:AL009665K01



5,6,7,30,32,34,40,41,43
4,5,6,7,11,12,20,21,22,23,24,27,28,30,36,38,40
4,7,23,27,28,30,31,32



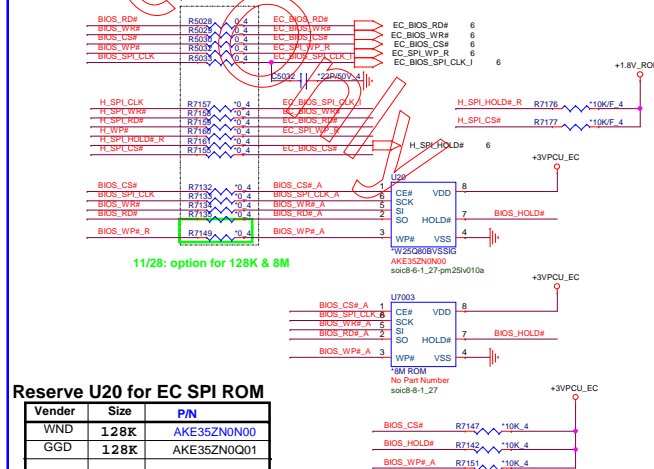
Smart adapter Type check



Adapter select

GPIO 42	adapter
High ==> DIS.	65W
Low ==> UMA	45W

Place them close U5001




Reserve U7003 for 8M SPI ROM

Vender	Size	P/N
WND	128K	AKE35ZN0N00
GGD	128K	AKE35ZN0Q01

Reserve U7003 for 8M SPI ROM

Vender	Size	P/N
WND	8M	NA

	PROJECT : X21 Quanta Computer Inc.		Revision 1
	Size Custom	Document Number EC (KB9028QF) CYROM	
Date: Tuesday, February 03, 2015		Sheet: 30 of 43	



Do Not add test pad on BATDIS_G signal

Do Not add test pad on BATDIS_G signal
Place this ZVS close to Diode away +VIN

Place this ZVS close to Far-Far away +VIN

15"

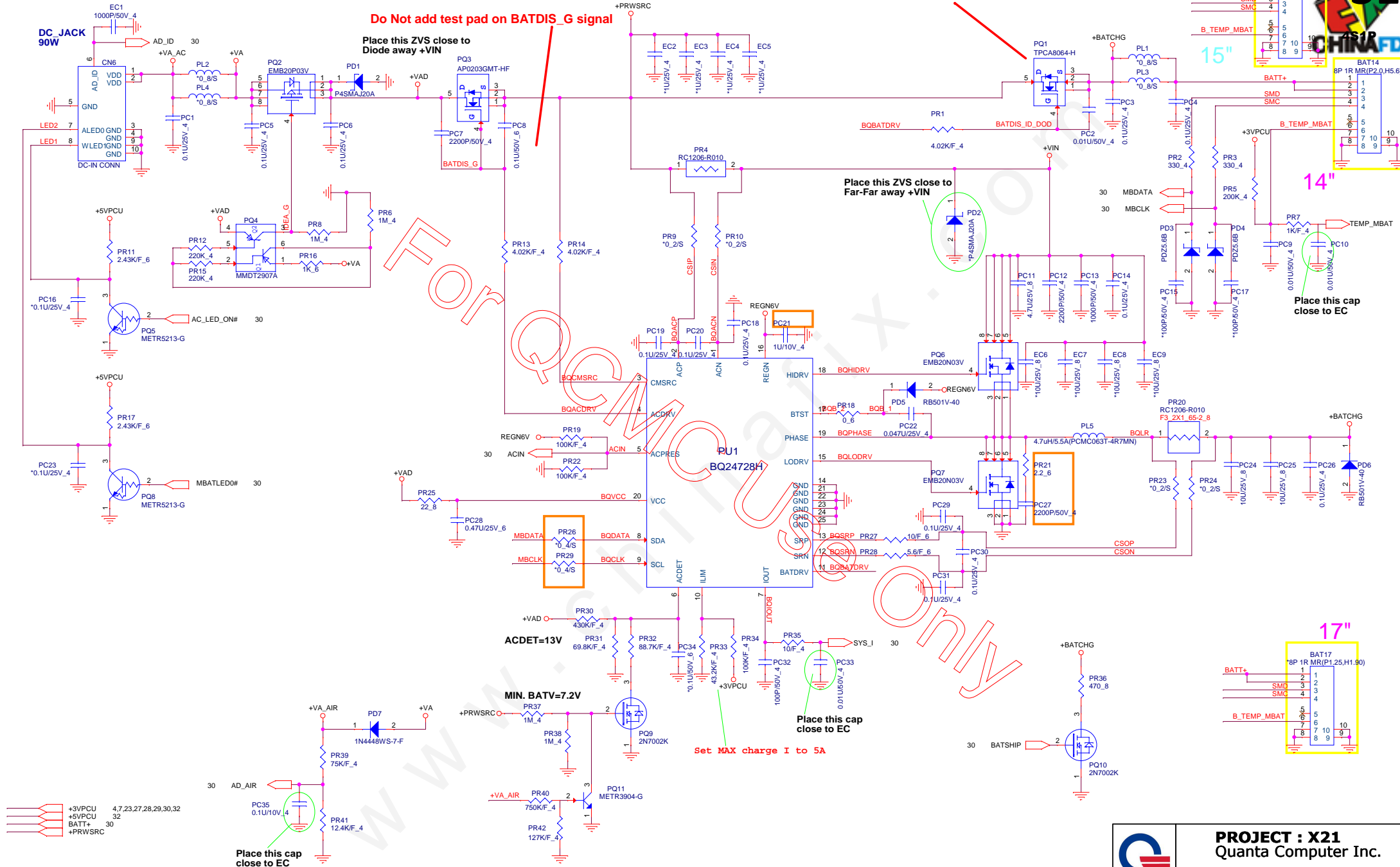
14"

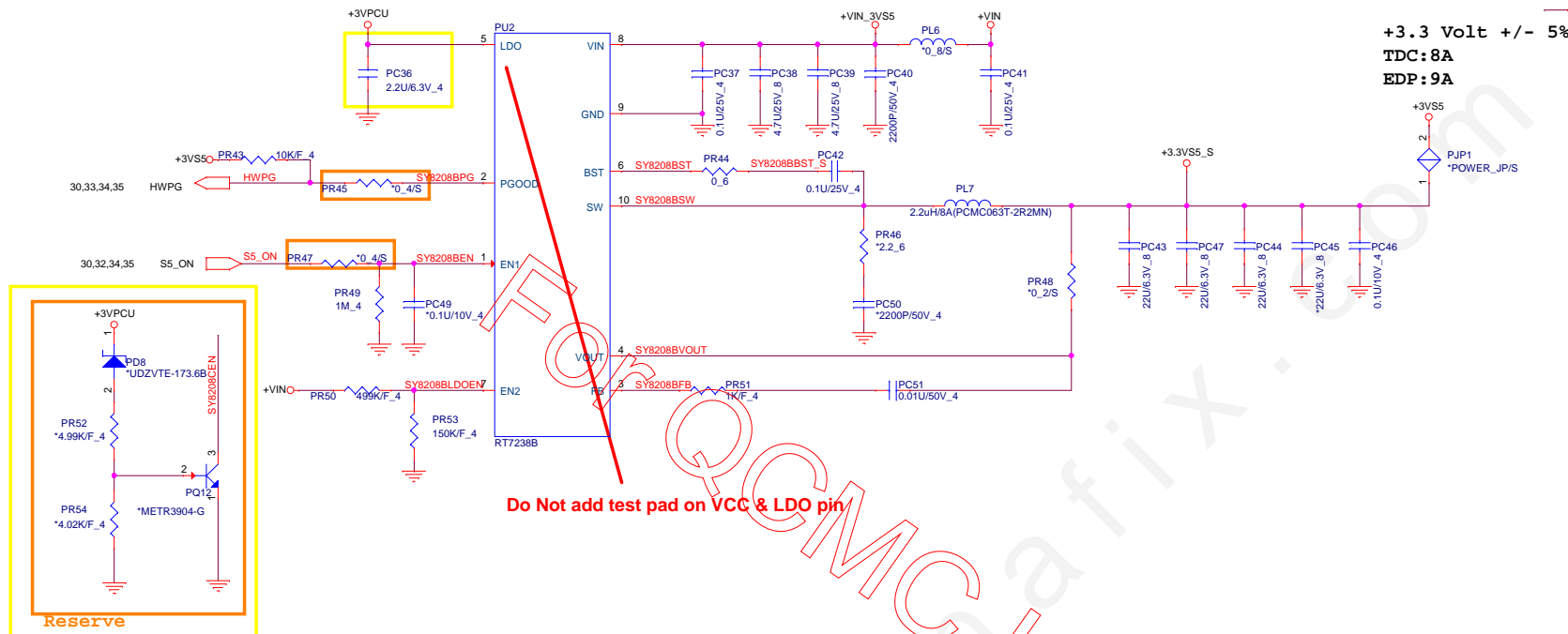
Place this cap close to EC

17"

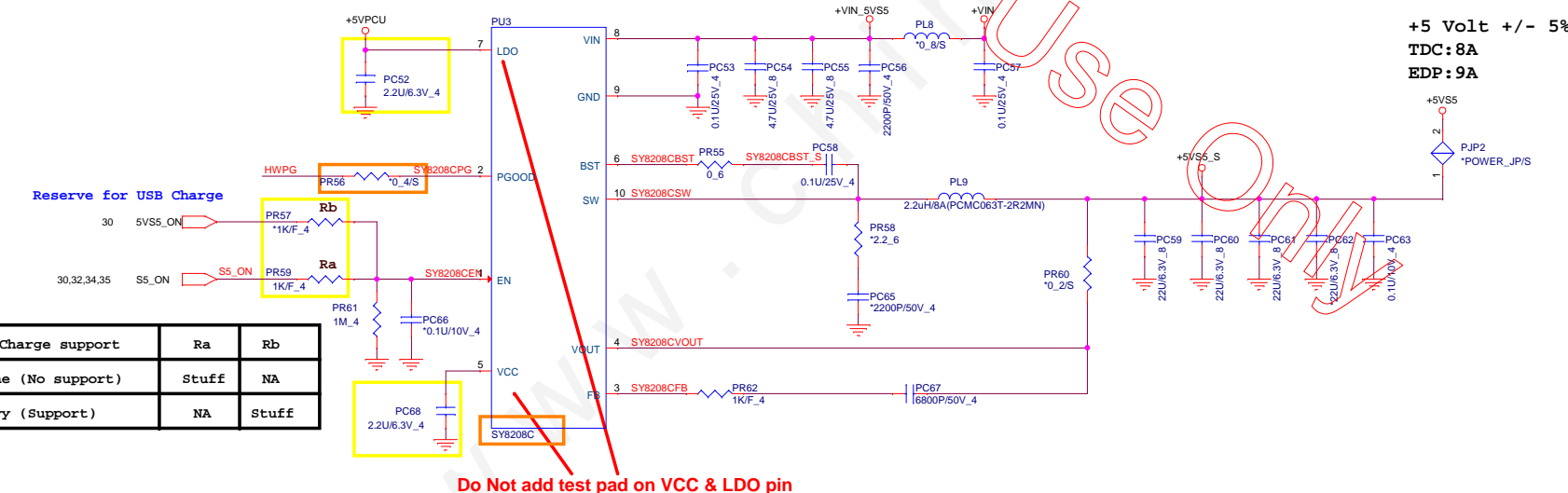
Set MAX charge I to 5A

Place this cap close to EC



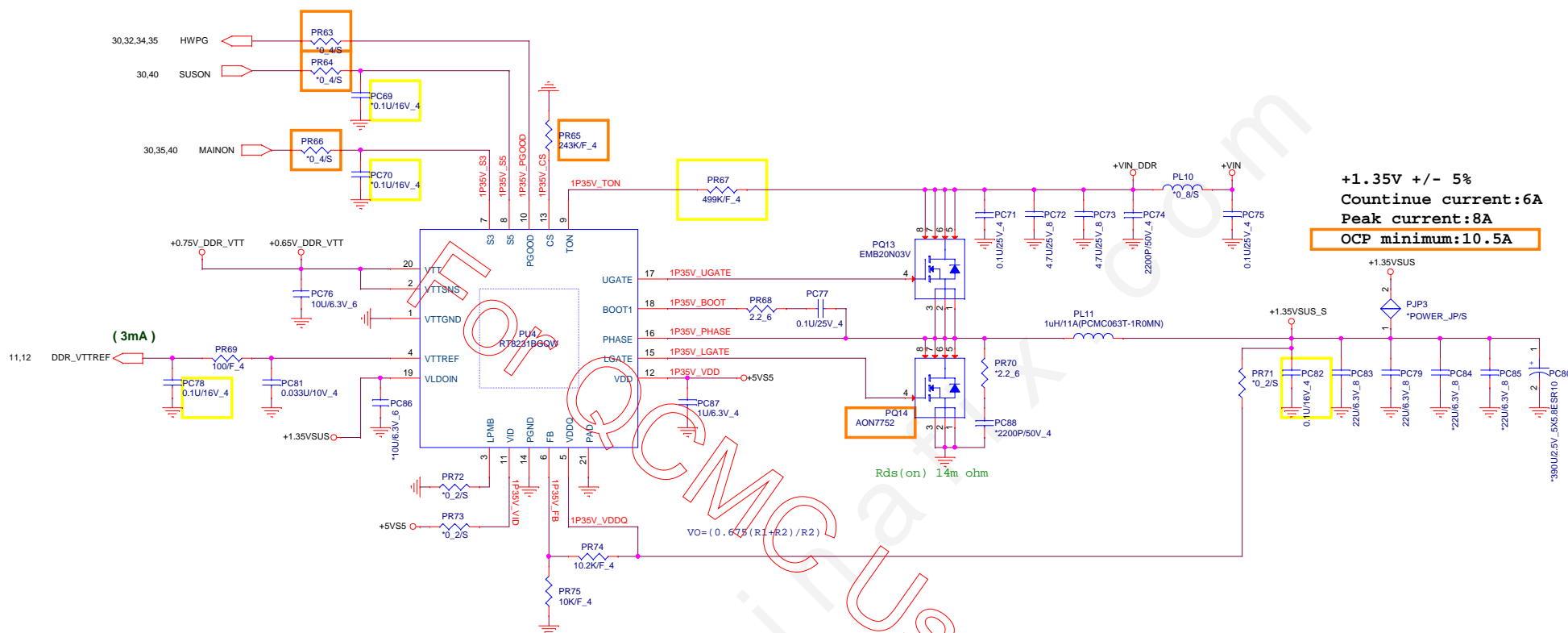


Do Not add test pad on VCC & LDO pin



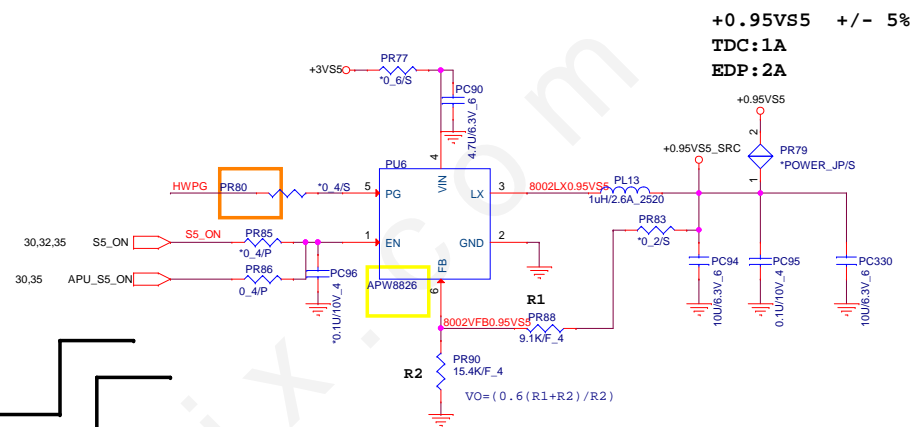
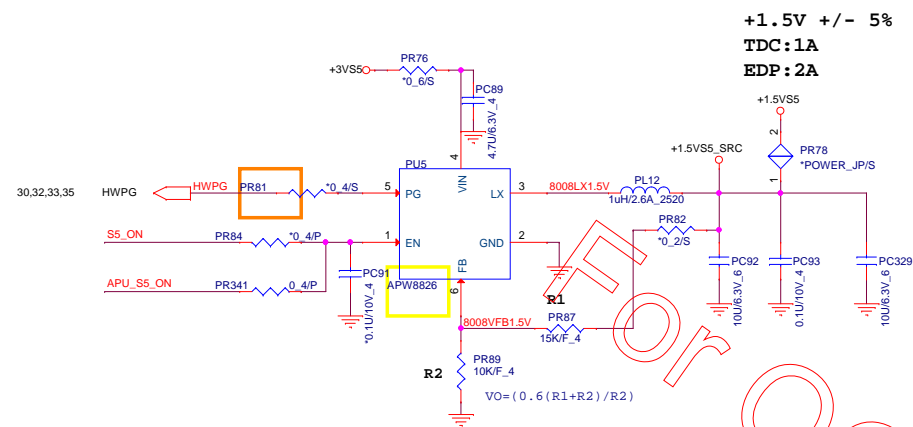
Do Not add test pad on VCC & LDO pin

USB Charge support	Ra	Rb
Vine (No support)	Stuff	NA
Envy (Support)	NA	Stuff

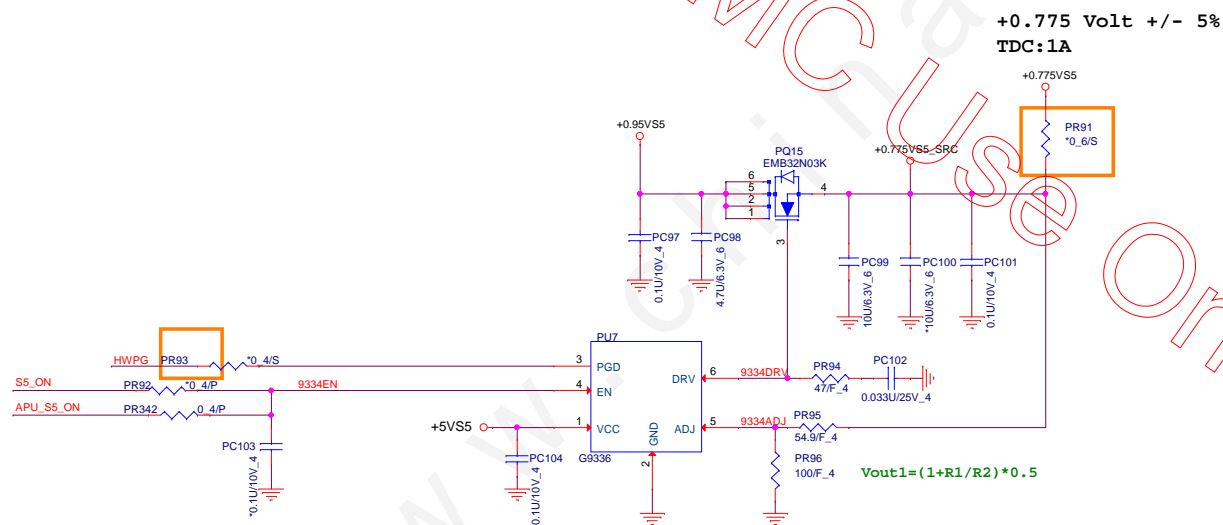


+1.35V +/- 5%
Continue current:6A
Peak current:8A
OCP minimum:10.5A

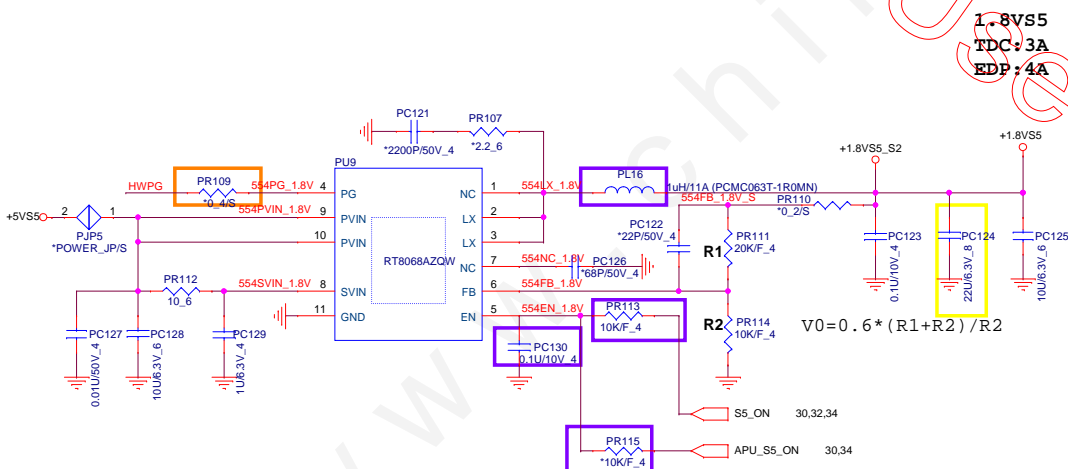
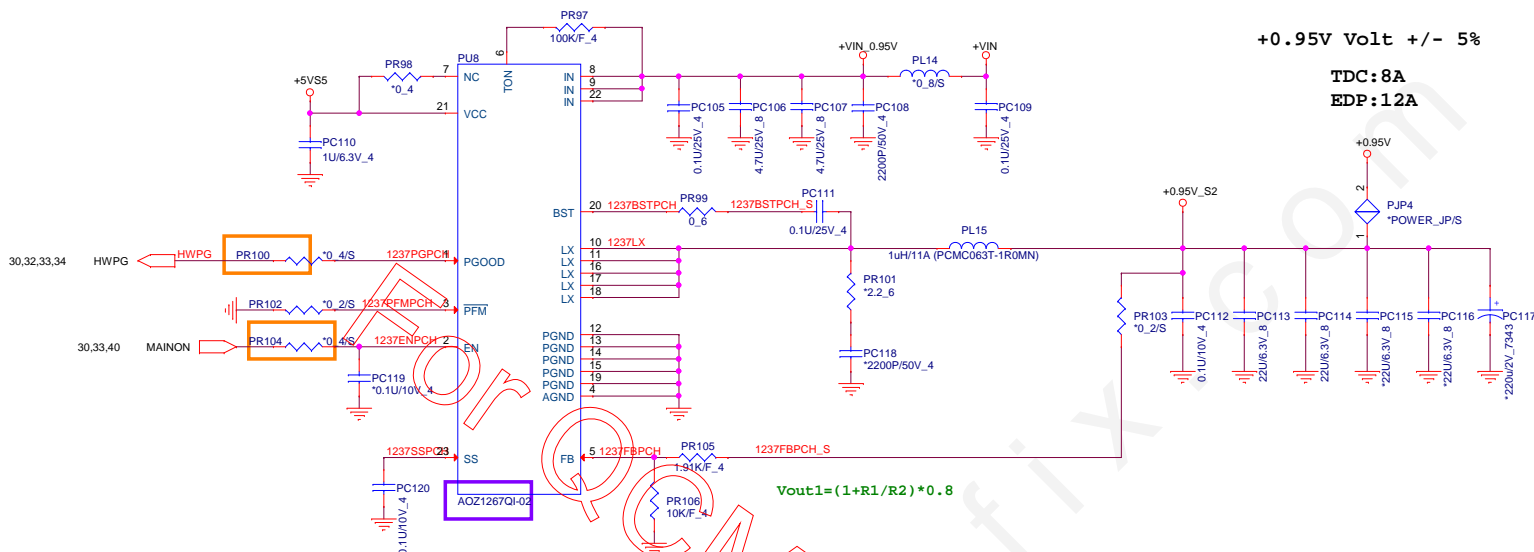
 +1.35VSUS 3,7,11,12

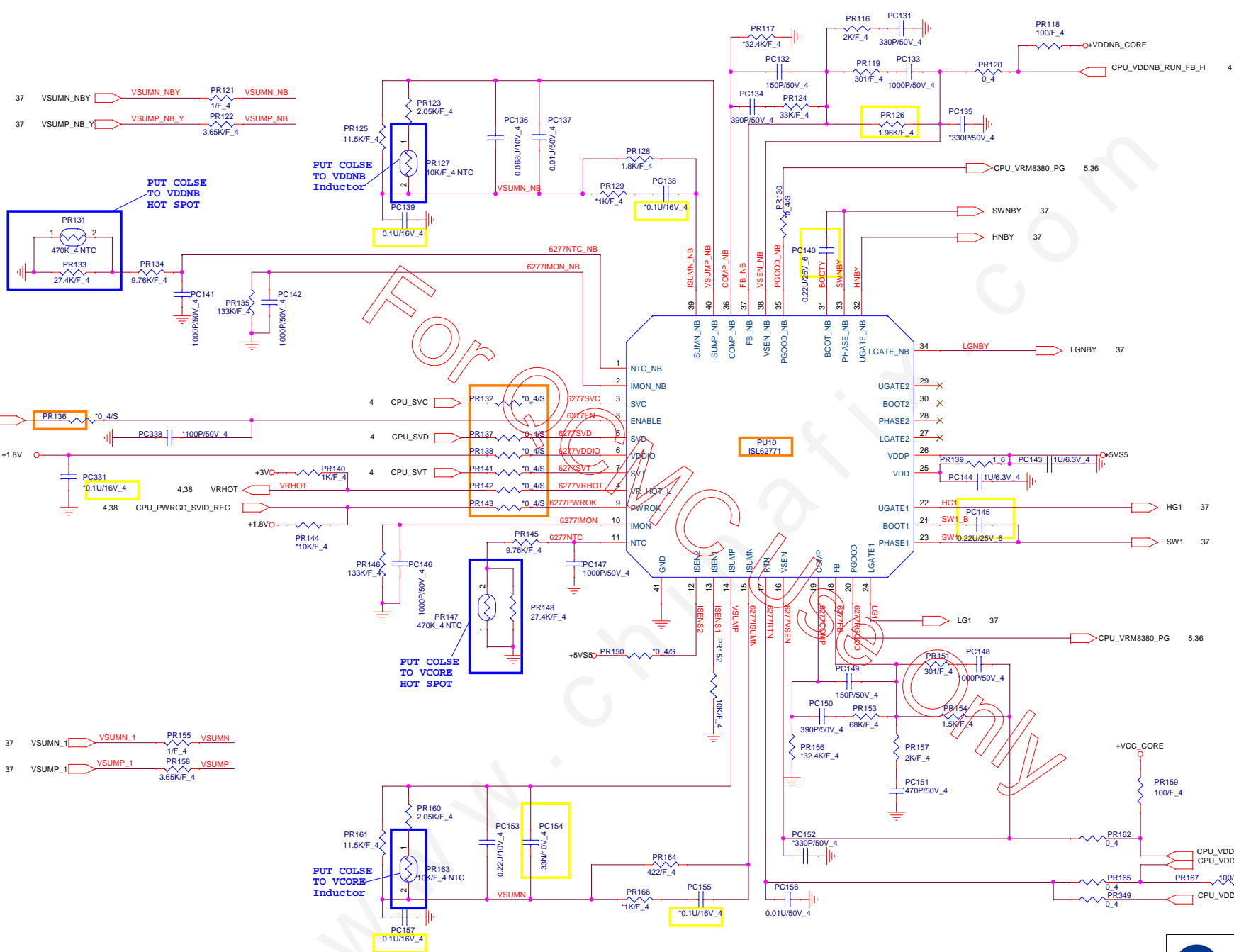


S5_ON
APU_S5_ON



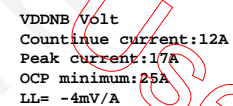
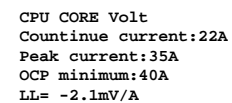
+VIN 21,25,27,31,32,33,35,37,39,40,41,42
+3VS5 5,6,7,29,30,32,40,41,43
+5VS5 23,28,32,33,35,36,38,40,41,43
+5VPCU 31,32

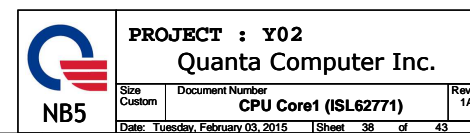
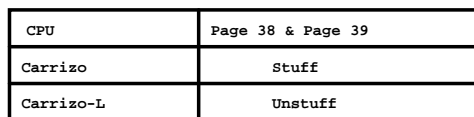


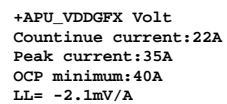


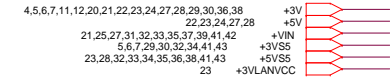
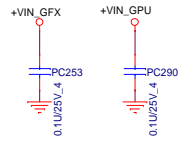
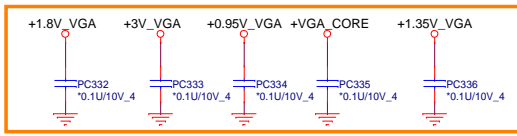
PROJECT : Y02
Quanta Computer Inc.

Size Custom	Document Number CPU Core1 (ISL62771)	Rev 1A
Date: Tuesday, February 03, 2015		Sheet 36 of 43

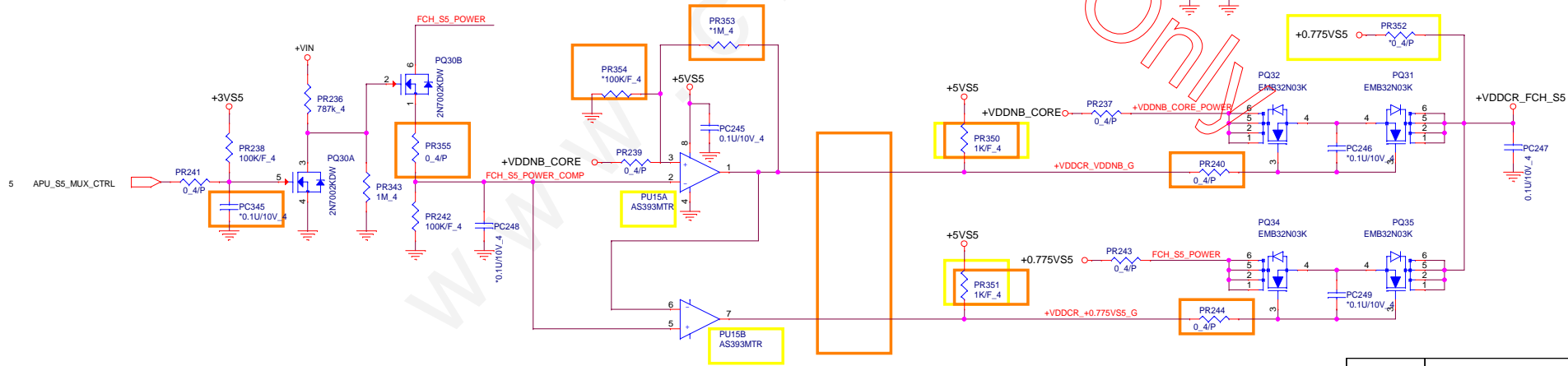
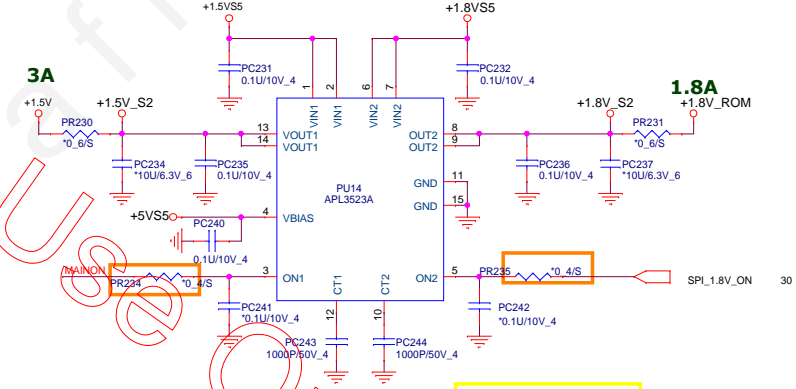
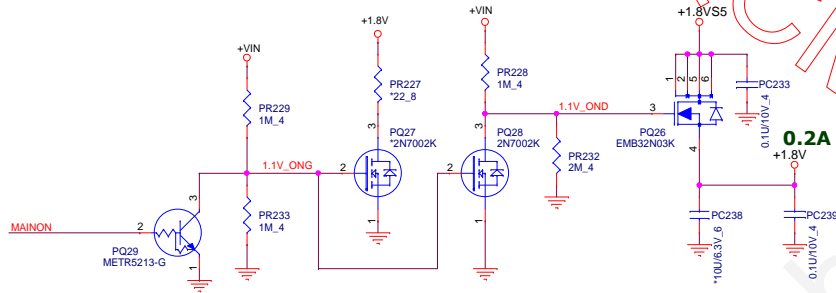
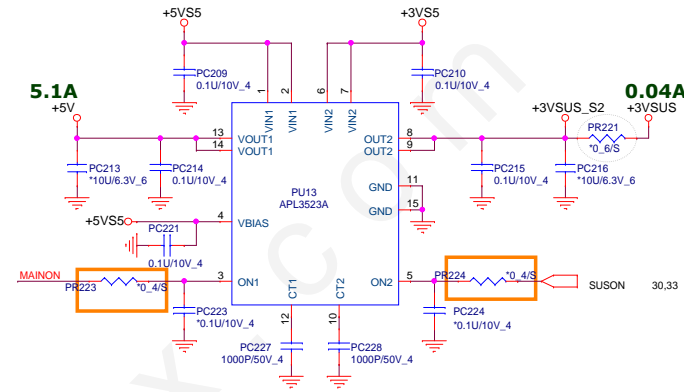
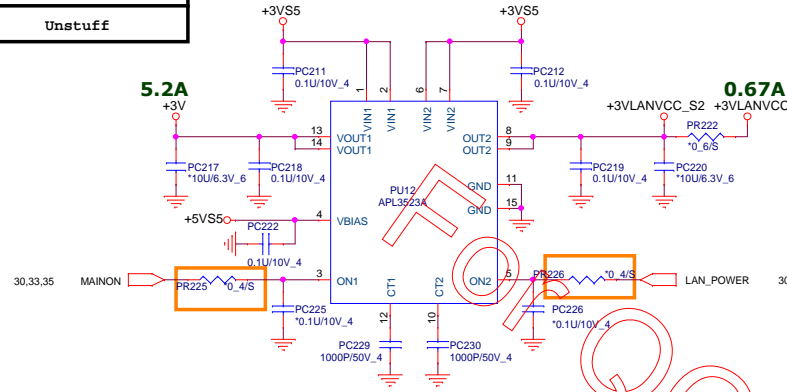




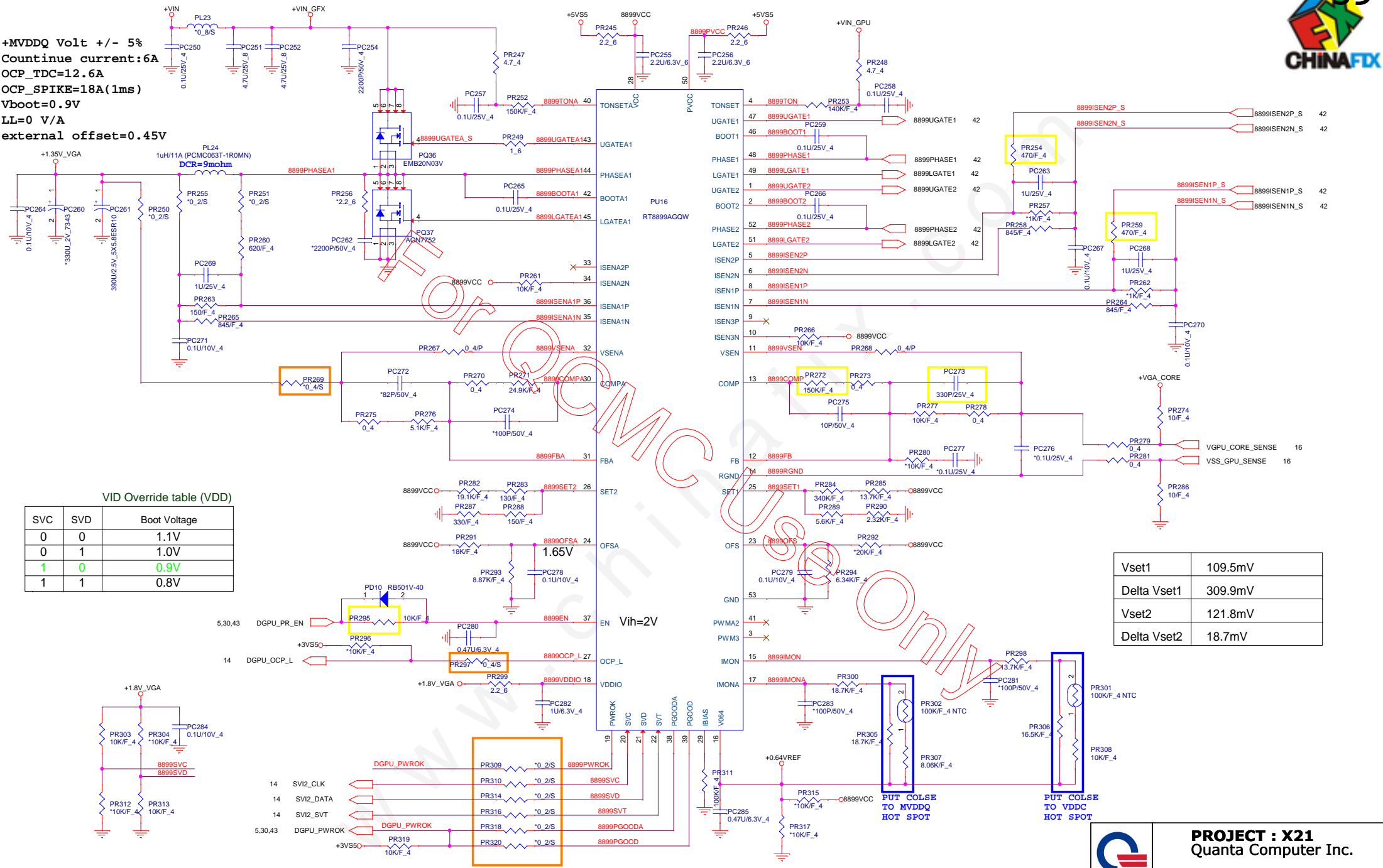




UMA only	Stuff
discrete	Unstuff



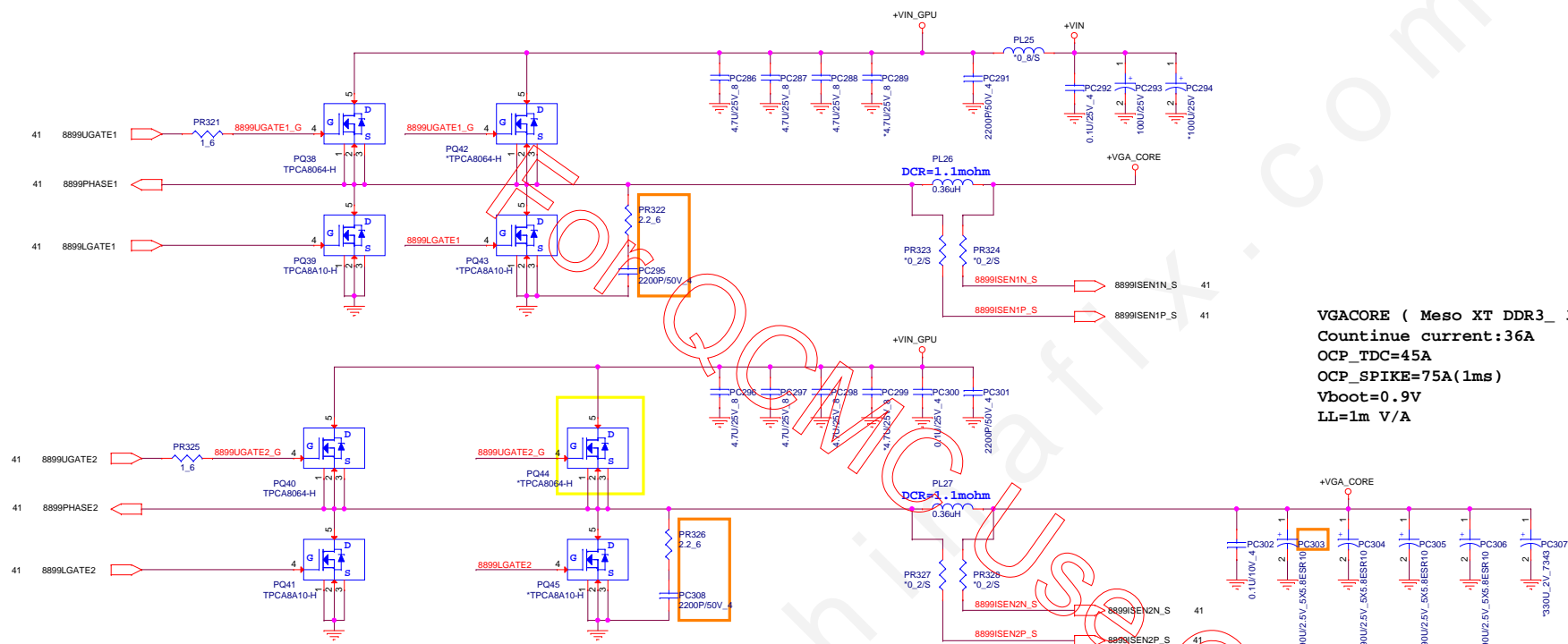
+MVDDQ Volt +/- 5%
 Countinue current:6A
 OCP_TDC=12.6A
 OCP_SPIKE=18A(1ms)
 Vboot=0.9V
 LL=0 V/A
 external offset=0.45V



VID Override table (VDD)

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

Vset1	109.5mV
Delta Vset1	309.9mV
Vset2	121.8mV
Delta Vset2	18.7mV



VGACORE (Meso XT DDR3_ 35W/53W(1ms))
 Countinue current:36A
 OCP_TDC=45A
 OCP_SPIKE=75A(1ms)
 Vboot=0.9V
 LL=1m V/A

